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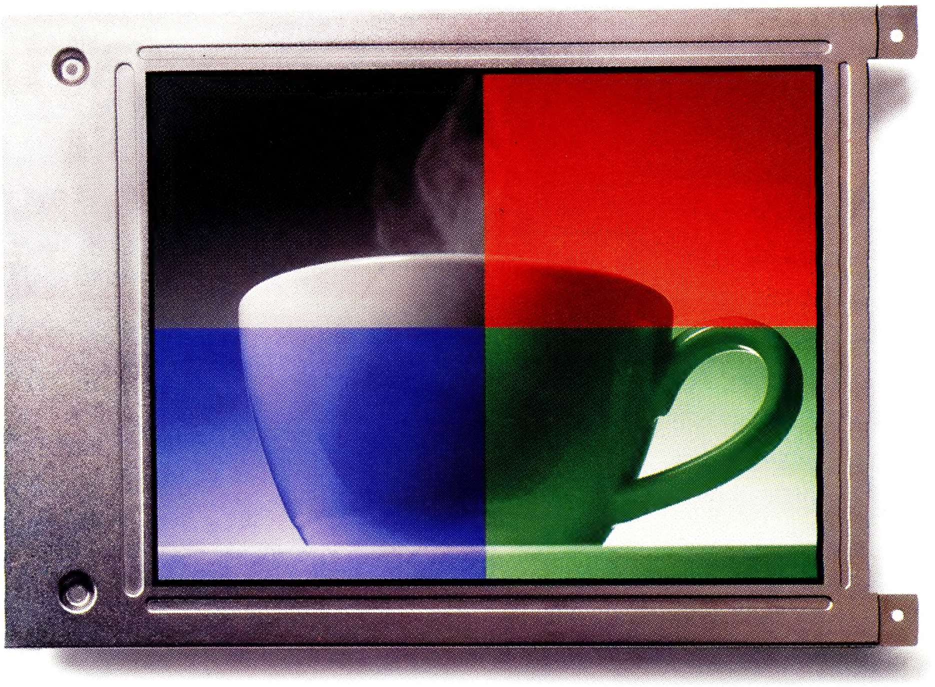
Quality in LCD production, that's Samsung's cup of tea.



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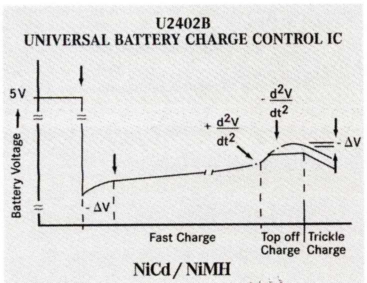

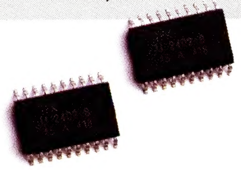

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COVER STORY

Microkernel and modular OSs 42

(Photo courtesy Microtec Research)

Home-automation buses 69

EDN READERS SELECT INNOVATOR AND INNOVATIONS OF THE YEAR

EDN's fifth annual campaign to pay tribute to innovative people and products has come to a close. We're proud to announce the winners that you chose from the field of finalists published in our February 2 issue. Award ceremonies will take place at the winning companies.

EDN congratulates all the nominations in this year's strong field of entries. **19**

EDN

DESIGN FEATURES

Microkernel and modular OSs

To produce more compact and adaptable code, software vendors are segmenting their operating-system kernels into modules surrounding a microkernel. As a result, they can offer a standard OS with custom configurability using minimal memory resources.

—Richard A Quinnell, Technical Editor **42**

Embedded Systems Conference

Sneak Preview: products from the Embedded Systems Conference. **57**

Home-automation buses: Protocols really hit home

Buses using wired and wireless technology—including IR, narrowband, and spread-spectrum communication—are bringing entertainment, security, and energy conservation to the home. But, even as several architectures vie for dominance, the industry keeps searching for that "killer application."

—Dan Strassberg, Senior Technical Editor **69**

Finding the keys to flyback power supplies produces efficient design

Many power-supply designers lack a good understanding of flyback-transformer power supplies. The reason is that energy delivered to the load stores in the transformer core itself and not in a separate inductor. A quick tutorial on flyback-power-supply design may help clear out some of the cobwebs.

—Brooks R Leman, Power Integrations Inc **101**

DMA module enhances μC CPU performance

Matching a μC's CPU performance to a particular application can be a tricky task. However, to enhance μC performance, a DMA module peripheral can offload many data-transfer tasks from the CPU—and help you defray overall system cost.

—Kevin Anderson, Motorola Inc **117**

STEP: a new standard for EDA tools

Surveys show that useful standards—not more bells and whistles—are what users need and want. Until now, EDIF and CFI, which offer limited usefulness, were the only standards available to meet those needs. Now, a new standard, STEP, has emerged and may well turn out to be exactly what users have been awaiting.

—Lars Celander, Institutet för Verkstadsteknisk Forskning **125**

OUT IN FRONT

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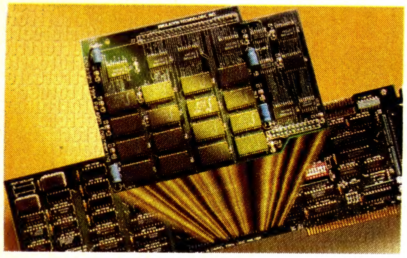

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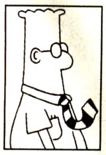

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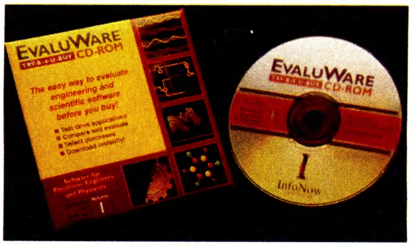
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8A switcher powers high-performance μP 88

Battery monitor draws 8 μA or less 90

Timer controls DSP-filter frequency resolution 92

EDN COLUMNIST

Warning: Your current fuzzy systems are only half fuzzy 179

The issue is defuzzification: what it is and what you can do with it.—*David Brubaker, Fuzzy-Logic Contributing Editor*

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Usable Gate		2LM:4K to 133K 3LM:7K to 232K	2LM:13K to 260K 3LM:22K to 500K	up to 300K	up to 350K	up to 780K	up to 1,110K
Pad Count		80 to 434	104 to 524	up to 444	up to 444	up to 524	up to 524
Number Of Base Array		16	24	–	–	–	–
Operating Voltage		5V	3.3V/5V	3.3V/5V		3.3V/5V	
Gate Delay (Fan out = 2)		205V	5V : 130PS 3.3V : 180 PS	190 PS	195 PS	5V : 160 PS 3.3V : 220 PS	5V : 193 PS 3.3V : 266 PS
Toggle Freq.		360 MHz	690 MHz	340 MHz	330 MHz	640 MHz	490 MHz
Power Consumption		3.7μW/gate/MHz	5V:3.6μW/gate/MHz 3.3V:1.3μW/gate/MHz	3.4μW/gate/MHz	1.9μW/gate/MHz	2.7μW/gate/MHz	0.6μW/gate/MHz
Output Drive (mA)		2,4,8 or 12	2,4,8,12 or 24	2,4,8,12 or 24		2,4,8,12 or 24	
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RAM	Max.bit Size	64K	128K	128K		128K	

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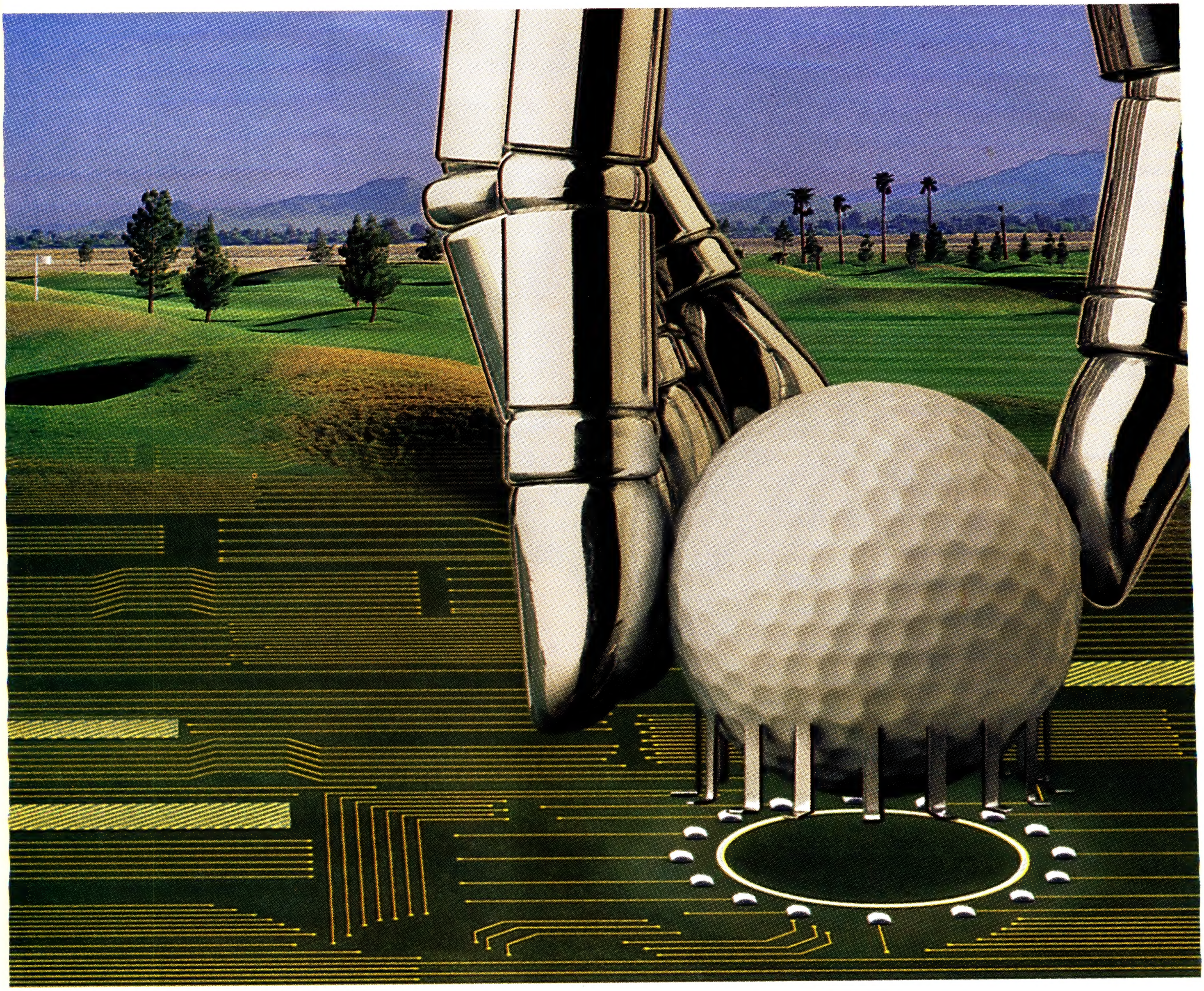

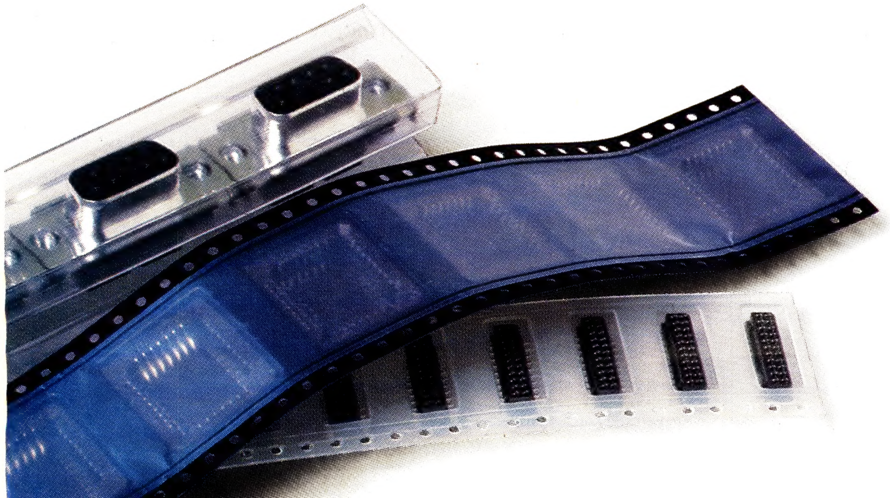

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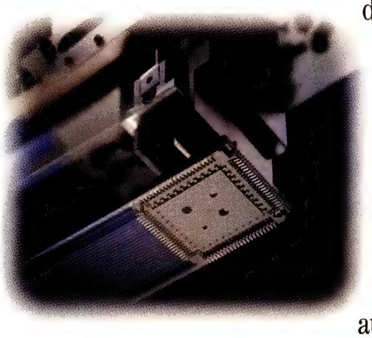

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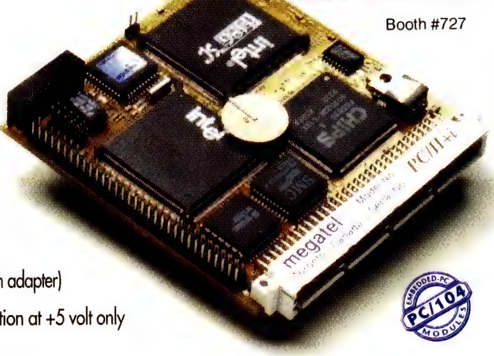

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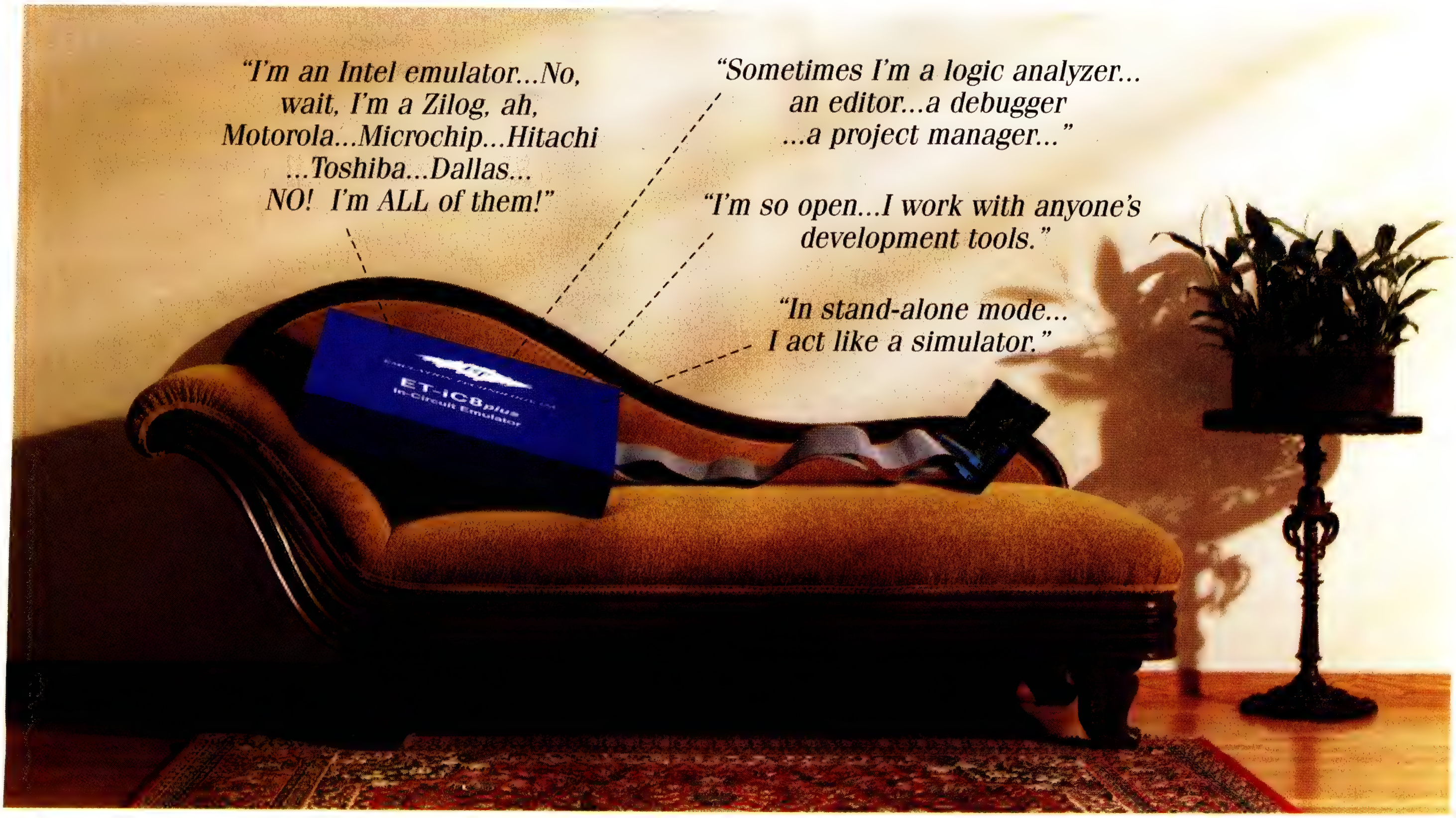

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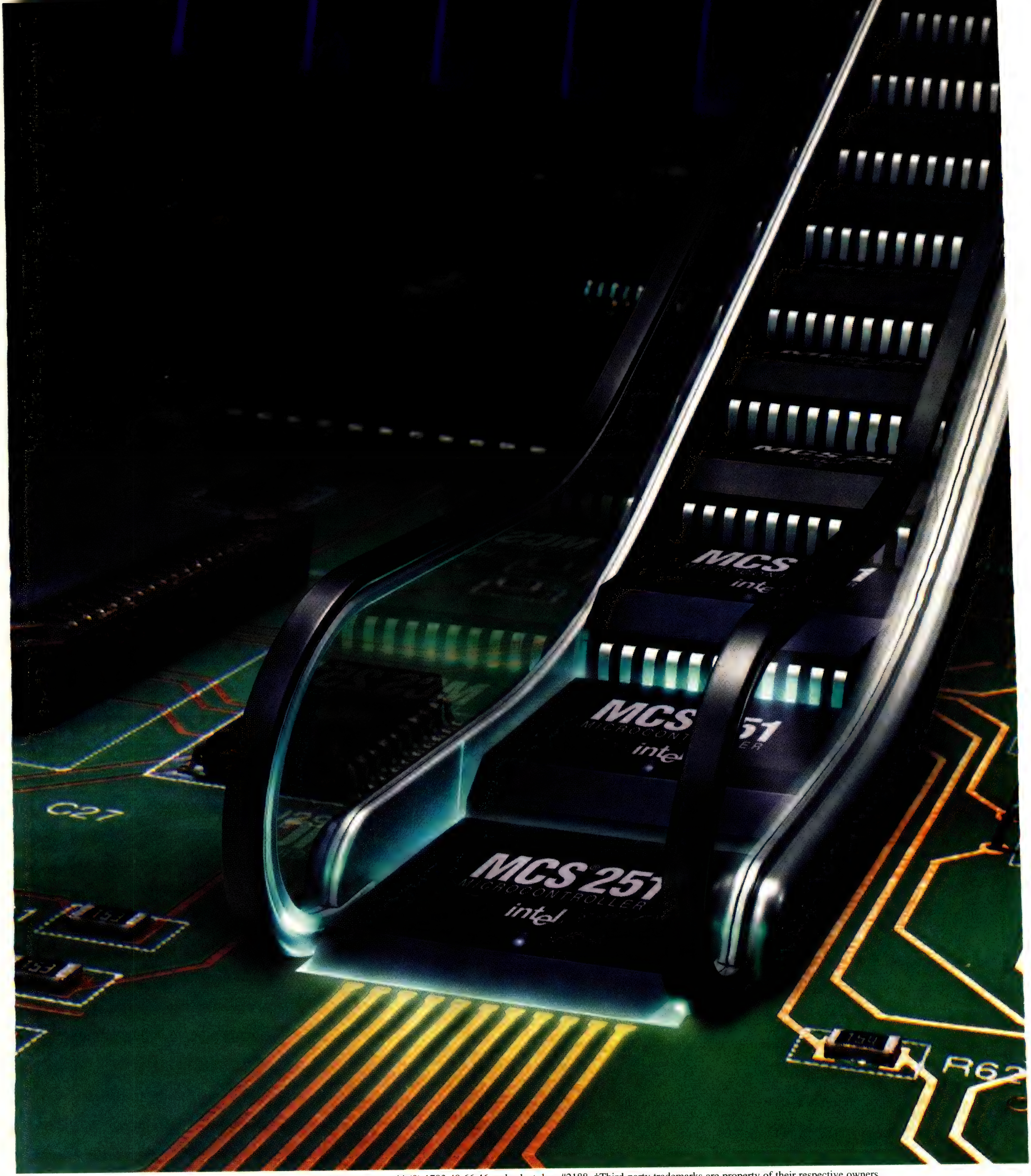

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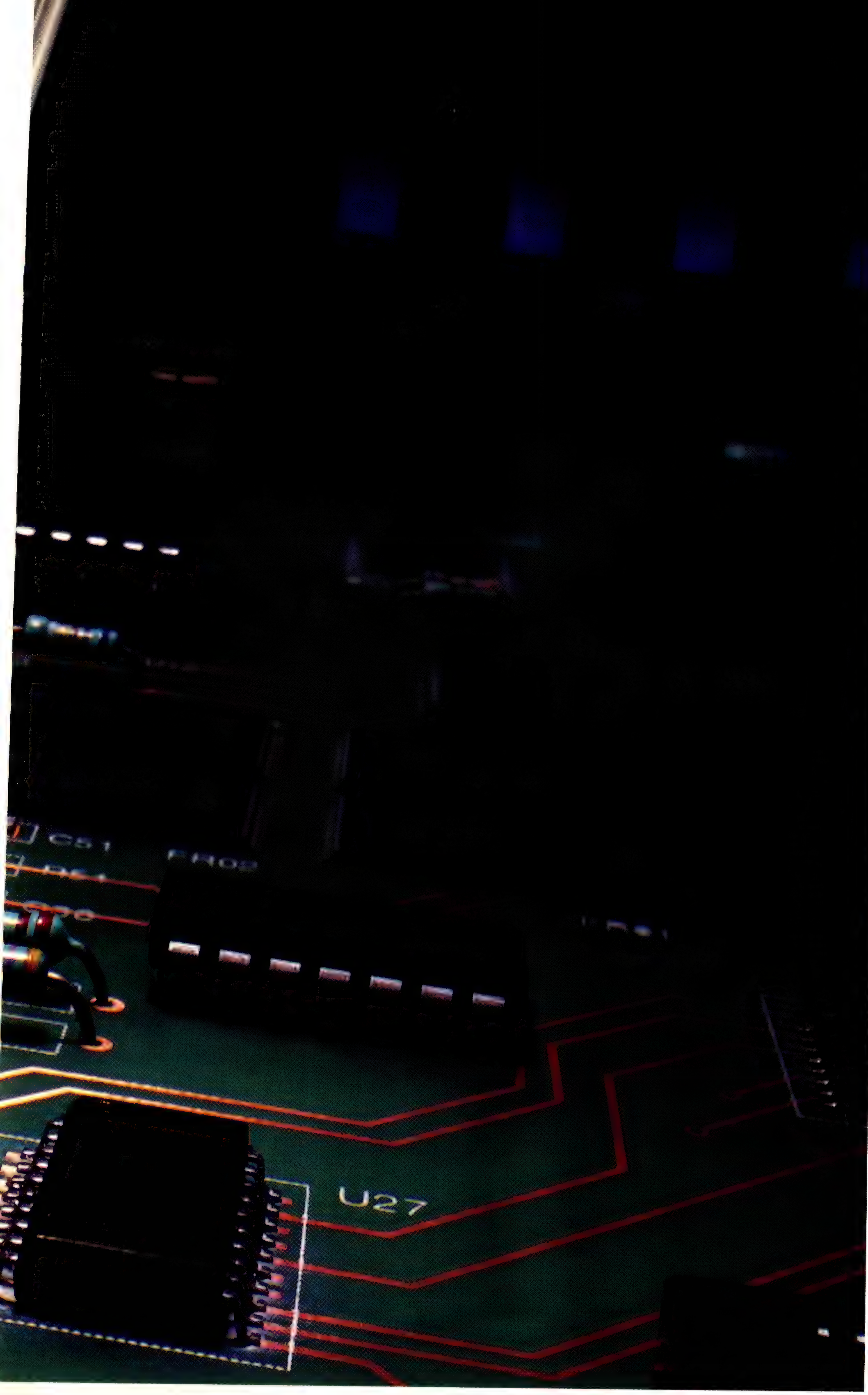

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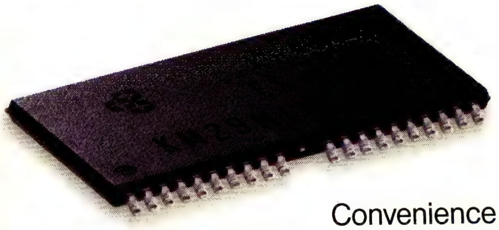

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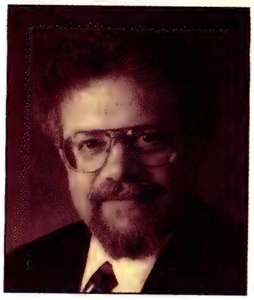
EDN READERS SELECT INNOVATOR AND INNOVATIONS OF THE YEAR

EDN's fifth annual campaign to pay tribute to innovative people and products has come to a close. We're proud to announce the winners that you chose from the field of finalists published in our February 2 issue. Award ceremonies will take place at the winning companies.

EDN congratulates all the nominations in this year's strong field of entries.



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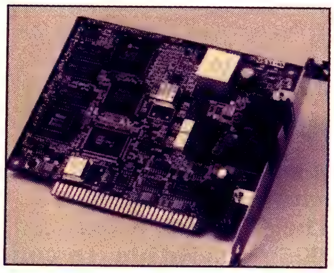

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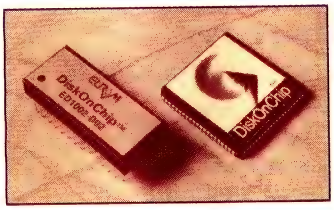


Low-gravity accelerometer provides dc response

Expanding from its ±50g-range, micromachined accelerometer technology, Analog Devices has introduced the ADXL05, a ±5g, full-scale device with 0.005g resolution. In contrast to piezoelectric devices, this IC provides a true-dc (gravity) response for use in precision-tilt and inertial-measurement systems, machine-health monitors, seismic instruments, medical-diagnostic equipment, suspension-control systems, and shipping-shock recorders. The monolithic IC includes sensor, modulator, demodulator, voltage reference, signal conditioning, and self-test circuitry.

The heart of the accelerometer is the sensing element. Rather than simply scaling down the 50g device, Analog's engineers designed a new suspended-beam, proof-mass geometry to achieve the factor-of-10 range decrease and

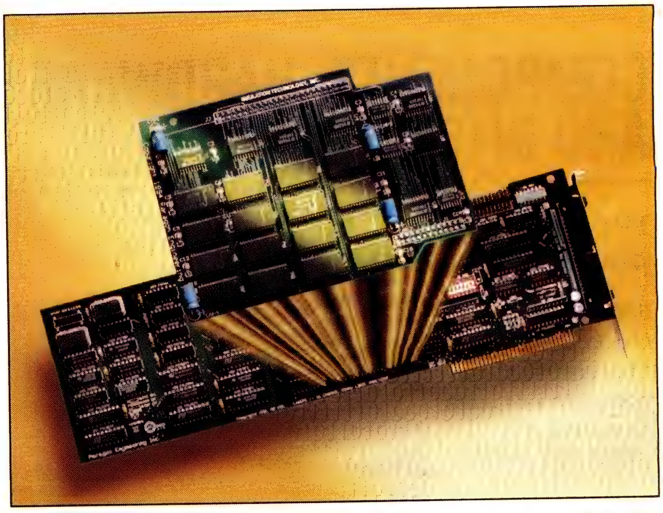
(continued on pg 22)

PC plug-in analyzers get 1M-word memory

Deep memory (1 Mbit/channel) is no longer the exclusive province of stand-alone logic-analysis systems. Emulation Technology has just introduced the ET-1MegPlus logic test system—a 16-channel ISA bus logic-analyzer plug-in board that clocks at 25 MHz with 1 Mbit of RAM behind each channel. (By using additional boards, the channel count can increase to 64; the speed can increase to 50 MHz if you monitor eight channels per board.) To be sure, the unit isn't nearly as fast as stand-alone, deep-memory logic analyzers, but, at $6295, it doesn't cost nearly as much. (It's $6595 configured as a generator of 16-channel digital patterns and two-channel analog waveforms.) And EEs who have PCs on their benches already have the analyzer's display and operator-interface subsystems.

The analyzer and generator differ only in their pods. By using alternate words in memory to define digital patterns and analog waveform values, the generator can simultaneously produce both 16-channel digital patterns and a pair of 8-bit-resolution analog waveforms. The analog outputs' frequency response is –3 dB at 750 kHz. The board, which comes with graphical-user-interface software, provides four levels of 16-bit-wide triggering (expandable to 64 bits) and can count 2^{64} events.

—by Dan Strassberg
Emulation Technology Inc, Santa Clara, CA, (408) 982-0660.
Circle No. 495



The small daughtercard of the ET-1MegPlus PC-based logic-test system contains 1M×16 bits of high-speed static RAM.

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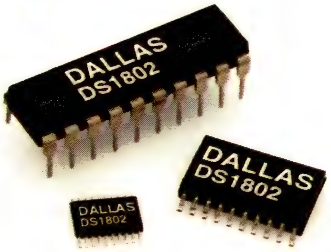

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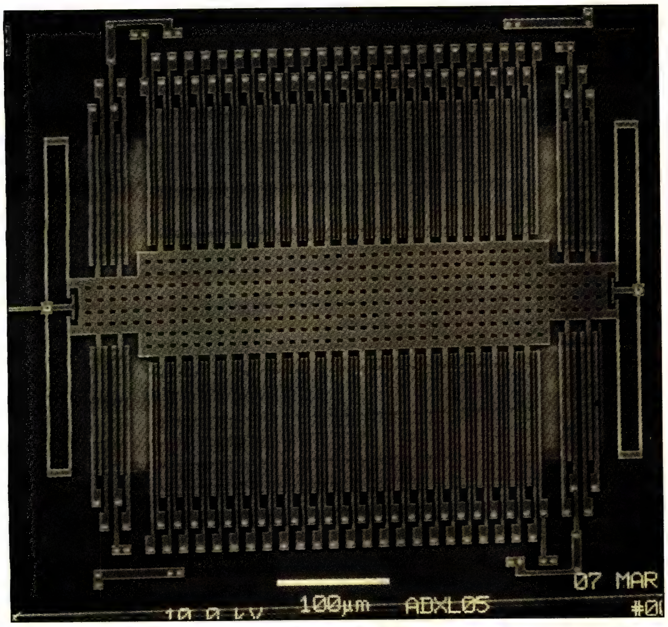
CIRCLE NO. 96

corresponding high sensitivity. The device comes in a hermetic 10-pin TO-100 metal can and costs $9.95 (OEM). —by Bill Schweber

Analog Devices Inc, Norwood, MA, (617) 937-1428. Circle No. 496



Analog Devices' ADXL05 accelerometer uses a new suspended-beam, proof-mass geometry.

Robotic leg controller wins Camaro in Philips Dream Machine Contest

A robotic leg controller patterned after an insect leg has won first place (the prize: a red Chevrolet Camaro) in Philips Semiconductors' Dream Machine Contest. Judges from Philips and *EDN* examined 97 contest entries to find the winner. Zhimin Ding at the Beckman Institute for Advanced Science and Technology, University of Illinois (Urbana, IL) created the design. The robotic controller, based on a Philips 87C552 µC, drives a two-jointed leg powered by gear motors. The leg not only provides motion, but also senses the best location for a firm footing on changing terrain. The 87C552's integral A/D converter measures joint location through potentiometers mounted on each joint and strain gauges mounted on the leg's motor shafts. Torque information from the strain gauges feed input into a servo-control loop with the µC's two PWM channels controlling the motors. Ding envisions grouping six of the legs together, tying the 87C552s together through their I^2C bus to create a complete robotic insect.

The second-place winner, created by John Harwood of Versatron Corp (Healdsburg, CA), is a 3-D mouse. The design employs an 8xC752 µC and uses the chip's A/D converters, internal timer, serial communications port, digital inputs, PWM, and low-power requirements to full advantage. Position sensing employs three Hall-effect sensors that measure relative position within a magnetic field. The mouse uses the earth's magnetic field for an absolute position reference. The second-place contest winner received a color notebook computer.

So many high-quality contest entries made picking one third-place winner impossible, so Philips awarded three prizes of a monochrome notebook computer. The three third-place designs are a tele-access authenticator, a hemoglobin analyzer, and a digital-lab power supply. The tele-access authenticator, designed by John Butler and Roger Davis of E-Systems ECI Division (St Petersburg, FL), permits secure telephone access. The authenticator employs a traditional challenge/response mechanism using the Data Encryption Standard (DES) algorithm to encrypt access codes. The design employs one 8xC752 µC as a commu-

(continued on pg 24)

DILBERT® by Scott Adams

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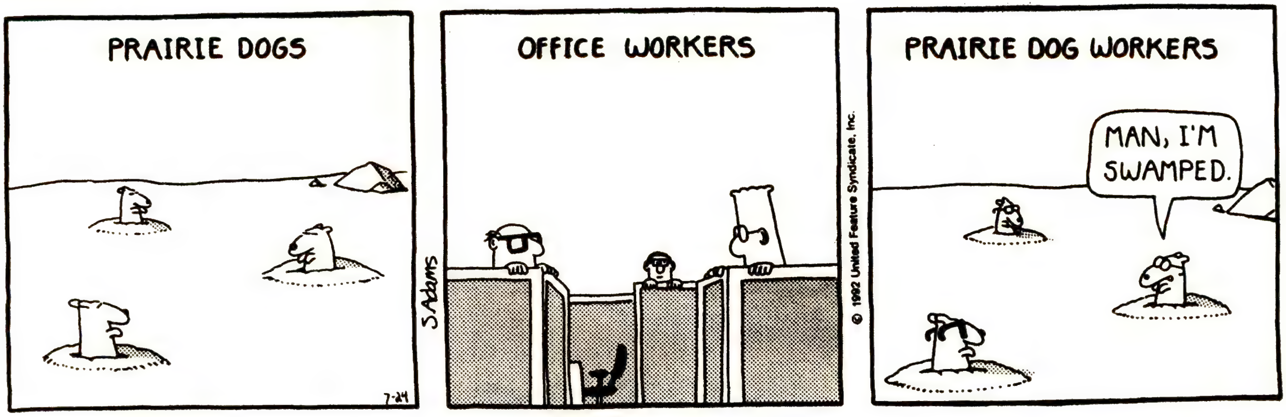

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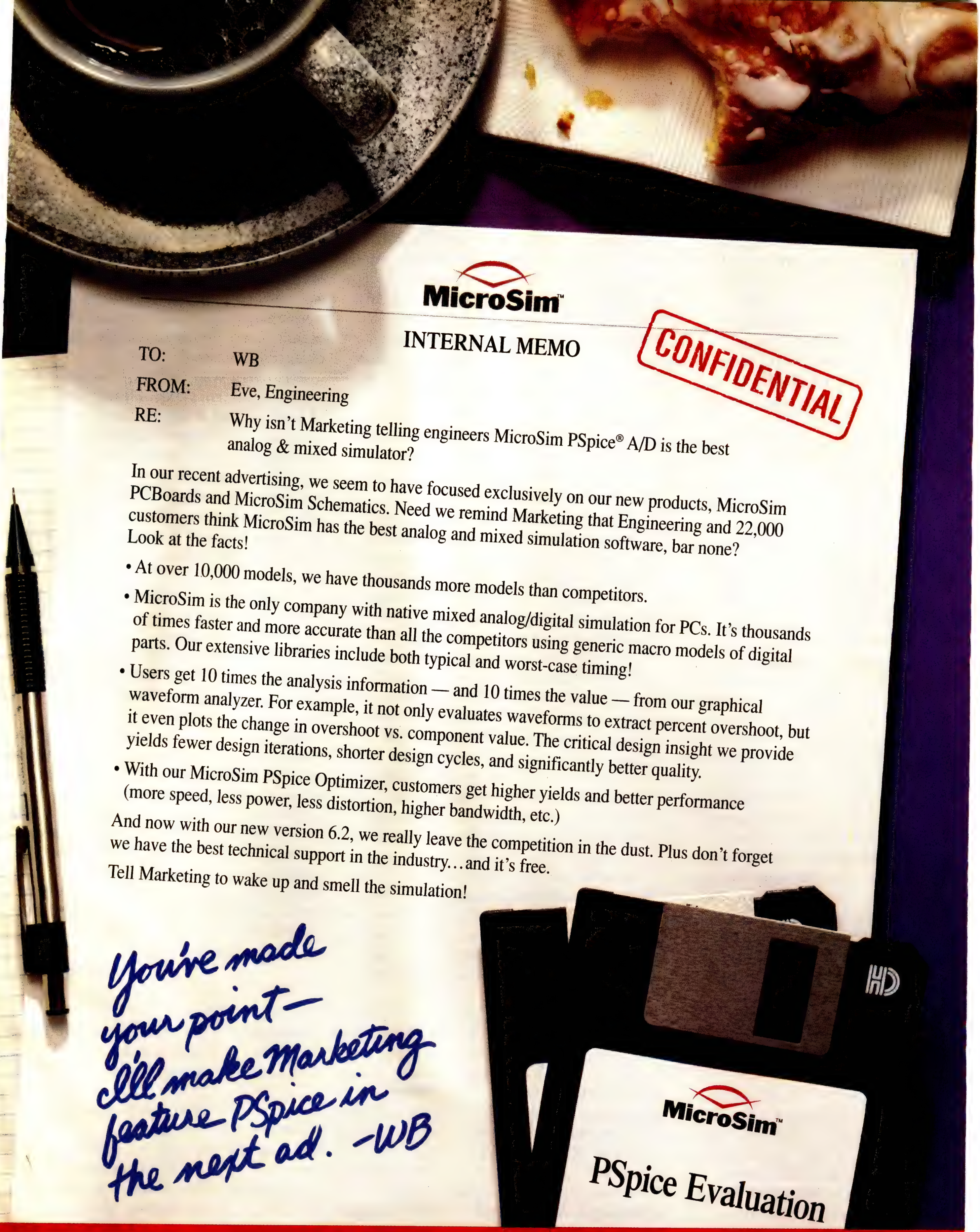**MicroSim**™

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CIRCLE NO. 204

nications processor, which generates and decodes dual-tone, multifrequency (DTMF) signals and one 8xC751 μC as a DES engine. The DTMF generator makes novel use of the μC's PWM, and the DES engine stuffs the entire DES algorithm into less than 2 kbytes of code.

The hemoglobin analyzer, developed by Dr J Patrick Eberly and Joseph Beitzinger of EQM Research Inc (Cincinnati), is a low-cost blood-analysis tool for use in developing countries. This third-generation product employs an 87C751 to reduce the parts cost and calibration requirements of earlier designs. A key attribute of the 87C751 was the device's 24-pin "skinny" DIP package. The size of the μC allowed the entire design to fit within an existing product enclosure. Operating the μC in idle mode whenever possible reduces the design's average current consumption to 12 mA and permits 40 hours of operation from the product's 9V battery. Another winning feature of this entry was the extensive mathematical analysis that allows the μC's code to perform complex calculations using fixed-point math.

Gordon Gleason of Web Technologies (Tucson, AZ) and Jerry Horn of Burr-Brown Corp (Tucson, AZ) developed the final third-place winner, a digitally controlled lab power supply. An 8xC752 μC forms the heart of the power supply's switching preregulator. Preregulation improves the supply's power efficiency by dropping the raw dc voltage supply to nearly the desired output voltage. A traditional linear-pass regulator then drops the remaining voltage and delivers relatively noise-free current. The 8xC752's A/D converter monitors the linear regulator's input and output voltage, and the μC's digital I/O and timer sections control the preregulator's silicon-controlled rectifier. Because the μC's 8-bit A/D converter doesn't provide sufficient resolution to give the power supply's voltage-adjustment pot an "analog" feel, the developers coupled an analog "dither" to the adjustment pot's output and then averaged 256 pot readings to get a finer resolution on the voltage setting. This technique improved resolution from 117 mV to better than 5 mV, effectively increasing the A/D converter's resolution to 12 bits.

—by Steven H Leibson

Philips Semiconductors, Sunnyvale, CA, (408) 991-3518.

Circle No. 497

Contest winner works out the "bugs" in winning μC contest entry

Studying cockroaches and stick insects helped 28-year-old Zhimin Ding create the winning design in Philips Semiconductors' Dream Machine Contest. Working with his academic advisor, Mark Nelson, PhD, Ding developed the robotic leg controller incorporating Philips' 87C552 μC after studying research on the insects' specialized legs. Stick insects reach out with a leg to find a branch or twig on which to place that leg—much as a robot's leg does in pick-and-place applications. Cockroaches are fast and agile, moving quickly over rough terrain, with front legs specialized for searching and rear legs specialized for providing forward thrust.

Until now, Ding says, robot legs have been symmetrical, and most robots have been one-legged. Ding's design will eventually control as many as six asymmetrical legs—much like the insects they copy. Further, the six legs provide a better strength-to-weight ratio than do one-legged designs. In addition, Ding's controller design adapts to its environment and "learns," so it does not have to be repeatedly reprogrammed for different environments.

Before winning the contest, Ding had accumulated a long list of academic accomplishments, beginning in his native China. There, Ding attended the University of Beijing, where he earned a bachelor's degree in control engineering and a master's degree in artificial intelligence. Five years ago, he came to the US and attended Georgia State University, Atlanta, to study psychology and neurophysiology. He conducted research on primates, including chimpanzees and monkeys.

But Ding was looking for an even wider academic experience, and his search ended with the Beckman Institute for Advanced Science and Technology at the University of Illinois in Urbana, IL. The Beckman Institute provided the right multidisciplinary mix for Ding, who is working toward a doctorate in neuroscience, which he hopes to attain in two years.

"Beckman Institute provided the right environment—a good mix of physiology, engineering, computation, robotics, and neuroscience—that I was looking for," Ding says. Ding also works at the institute as a research assistant.

Ding's interest in things scientific began in China, where, as a 10-year-old, he began building transistor radios because they were too expensive to buy. He still plays with "toys," he says, listing his hobbies as building radio-controlled airplanes and playing the violin. He hopes to pursue a career as diverse as his education has been—one that will allow him to combine his disparate interests.

—by Fran Granville

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OP293	100 µV V_{OS}, 20 µA at 2-V Supply
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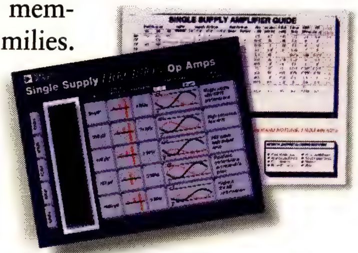

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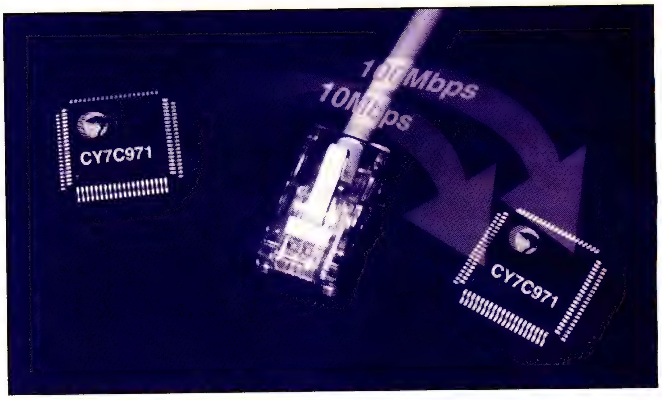
CIRCLE NO. 17

Ethernet transceiver transmits at 100 Mbps over UTP cable



The Cypress CY7C971 100BaseT4 transceiver operates at dual speeds.

Cypress Semiconductor's new CY7C971, a dual-speed (10- and 100-Mbps) Ethernet transceiver, allows data transmission over installed category 3, 4, and 5 unshielded twisted-pair (UTP) cable. The device supports the 100BaseT4 Fast Ethernet standard, along with 10BaseT and 10BaseT full-duplex standards. It allows seamless integration of 100-Mbps equipment into 10-Mbps networks. It provides an economical way of building dual-speed 100BaseT4/10BaseT adapter cards, repeaters, bridges, routers, and switches.

The CY7C971 incorporates adaptive equalization, clock recovery, encoder/decoder functions, and transmit and receive filters into a single chip. The chip comes in an 80-pin PQFP, which conforms to the width of an RJ45 connector.

In addition, the CY7C971 implements "auto-negotiation," or the "NWay algorithm." This feature allows the device to configure itself to the highest available speed of the three operating modes—100 or 10 Mbps or 10 Mbps full duplex—with one RJ45 connection and without management intervention. Auto-negotiation lets you plug dual-speed devices into standard 10BaseT networks; when you upgrade your network to 100 Mbps, the CY7C971 will transparently switch to the highest speed.

The device's on-chip adaptive equalizer senses the length of the cable over which the data are transmitting on every frame. The frame-to-frame adaptation compensates for temperature and environmental variations that change the attenuation characteristics of the cable during normal operation. The equalizer can handle worst-case cables, such as category 3 polyvinyl-chloride-insulated cables.

The chip's analog-based equalizer delivers performance twice as fast as that of DSP-based equalizers, according to the company. The lower latency lets you add ports in stackable hubs and allows the transceiver to be used for Class 2 repeater applications. Price is $25 (1000).

—by John Gallant

Cypress Semiconductor Corp, San Jose, CA, (408) 943-2600. **Circle No. 498**

OPINION...

Cyrix poses M1 against Intel P6

Cyrix has begun shipping initial samples of its M1 µP. The M1 is internally a RISC µP, but it can run X86 code in native mode. Although industry observers have so far referred to the M1 as Cyrix's answer to Intel's Pentium, Cyrix is calling the M1 a sixth-generation X86 µP. Thus, Cyrix is positioning M1 against Intel's P6, not against the Pentium.

Cyrix's argument for calling M1 a P6 alternative is that the M1's performance is equivalent to that of the P6 at the same internal clock frequency. Cyrix's internal tests indicate that M1 has a 2.2-times performance improvement over Pentium, using PC-application benchmarks. Cyrix points out several internal-architectural features of the M1 that are similar to those of the P6. Additionally, Cyrix claims that P6 performs internal RISC operation translation to run X86 code.

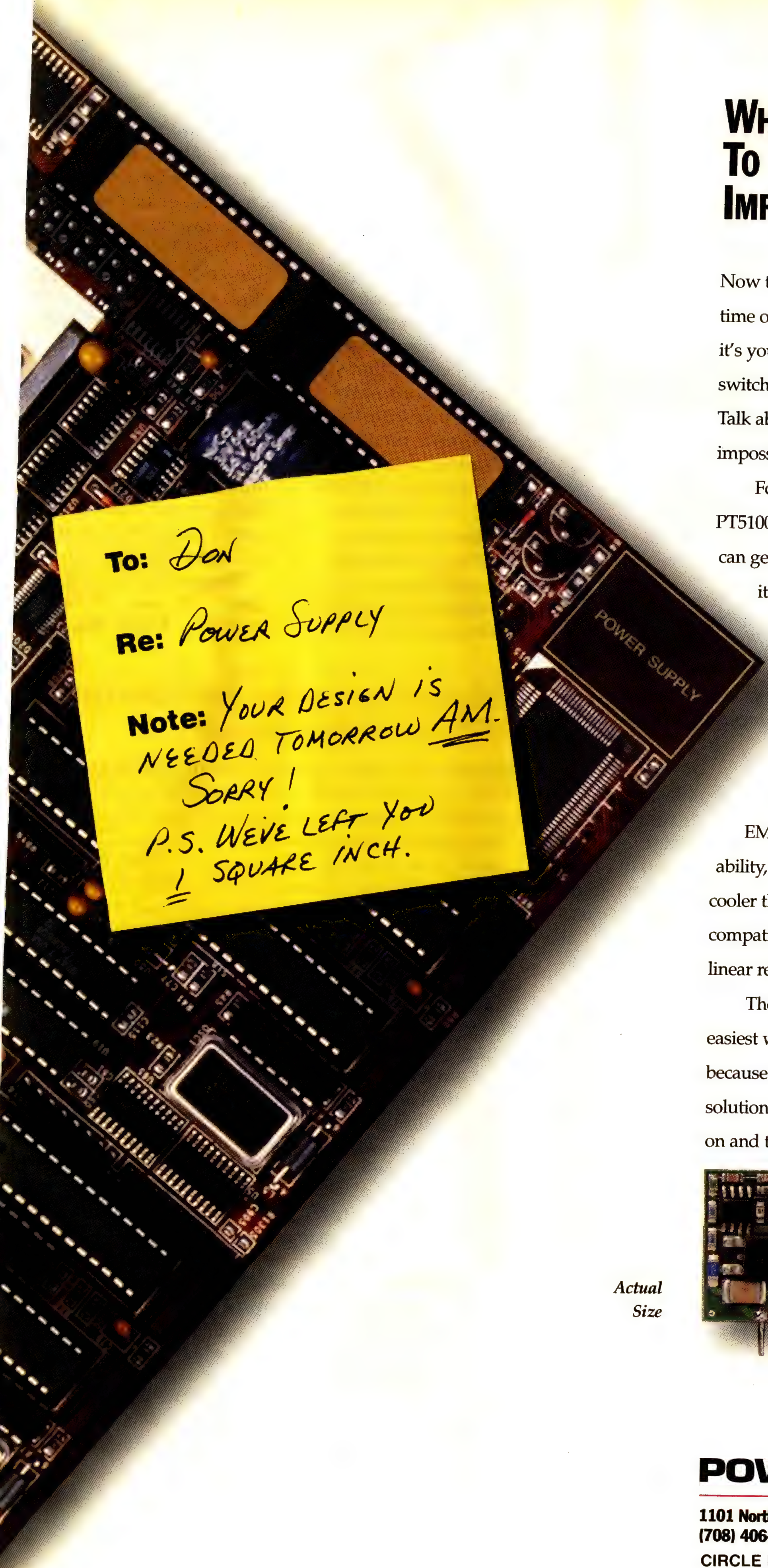
Cyrix admits that the M1—with one more instruction than the Pentium—does not have the full P6 instruction set. But most PC applications are written for 386 and 486 µPs. Independent software vendors address the installed base. Even for the next few years, most applications may not even use the full Pentium instruction set. Thus, Cyrix contends the M1's performance running this code makes the M1 a sixth-generation X86.

Cyrix is offering two versions for sampling: the M1 in a Pentium-socket-compatible package and the M1-SC in a DX4-socket-compatible package. The M1, a 3.3V CMOS design, is compatible with all Pentium chip sets, including those from Intel. Current samples operate at 90 MHz; however, Cyrix plans to ramp up production to 100-, 120-, and 133-MHz versions.

In-Stat views Cyrix's touting the M1 as a sixth-generation µP as an aggressive marketing move. How the market accepts the device remains to be seen. Cyrix is offering considerably higher performance in a Pentium package. Making it available in a DX4 package gives Cyrix added leverage.

—by Tony Massimini, Senior Market Analyst for Micro Logic, In-Stat

In-Stat, Scottsdale, AZ, (602) 483-4440. **Circle No. 499**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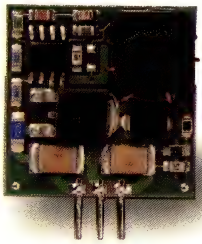
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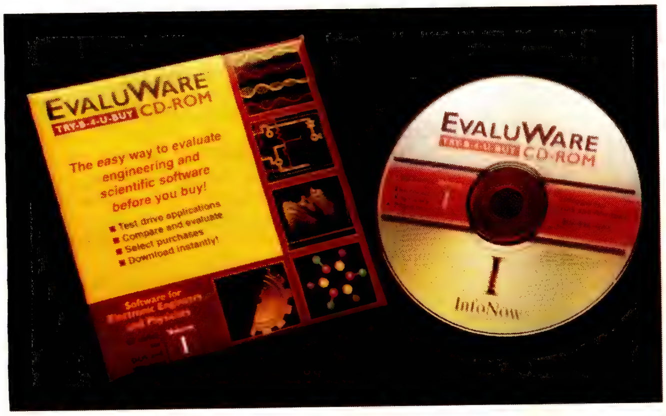

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—by Dan Strassberg

InfoNow Corp, Boulder, CO, (800) 842-4669.
Circle No. 500

UK company files suit for software-copyright infringements

UK-based Flomerics has instituted an action for copyright infringement and trade-secret misappropriation against US-based Fluid Dynamics International (FDI). Flomerics claims that FDI, in producing a product called Icepak, has misappropriated and copied key components of Flomerics' Flotherm thermal-analysis software and reference manual.

Icepak, which FDI released last year, targets essentially the same applications as Flotherm does. In a formal complaint, Flomerics claims that significant portions of the graphical user interface and reference manual for both Flotherm and Icepak are identical or strikingly similar. The similarities relate to nomenclature, instructions, command and menu language, and the content and sequence of textual screen displays. The complaint cites around 400 examples of copying and even includes a formula error that Flomerics subsequently corrected. David Tatchell, CEO at Flomerics, says FDI's copying is so flagrant and pervasive that Flomerics has to take action.

US authorities have entered a temporary restraining order prohibiting FDI from secreting or destroying any documentation relating to Flotherm or Icepak programs and reference manuals.—by Brian Kerridge

Flomerics, Hampton Court, UK. +44 181 941 8810. **Circle No. 501**

Chip set encodes and decodes MPEG-2 video frames

IBM Microelectronics has announced two video chips, an encoder and a decoder, that work together to compress and decompress MPEG-2 video. Both chips employ IBM's 0.5-µm, 3.3V, CMOS 5L technology. The encoder comes in a 304-pin CQFP and costs $700 (50). The decoder comes in a 208-pin CQFP and costs less than $35 (OEM).

The encoder chip compresses, or encodes, data to transmit and store digital video pictures, frame by frame. It suits high- and low-end digital MPEG-2 applications because it can compress I-frame video in real time. The encoder operates in 4:2:2 chroma format in CCIR 601 (720×480-pixel) resolution as well as in 4:2:0 mode. The 4:2:2 format provides better color definition for studio-quality video. The device also features a built-in 54-MHz RISC µP, which allows the chip microcode to adapt to an application's requirements. It provides a direct interface to industry-standard DRAMs and boasts a scalable architecture.

The MPEG-2 decoder supports IPB frames in 4:2:0 mode and I-frame only in 4:2:2 mode. It also supports sustained decompression rates greater than 40 Mbps for I-frames and as much as 15 Mbps for IPB frames. The decoder has a 40-MHz RISC µP and a memory bus that allows it to work with 1, 2, or 4 Mbytes of DRAM.—by John Gallant

IBM Microelectronics, Fishkill, NY, (800) 426-0181, ext 1503. **Circle No. 502**

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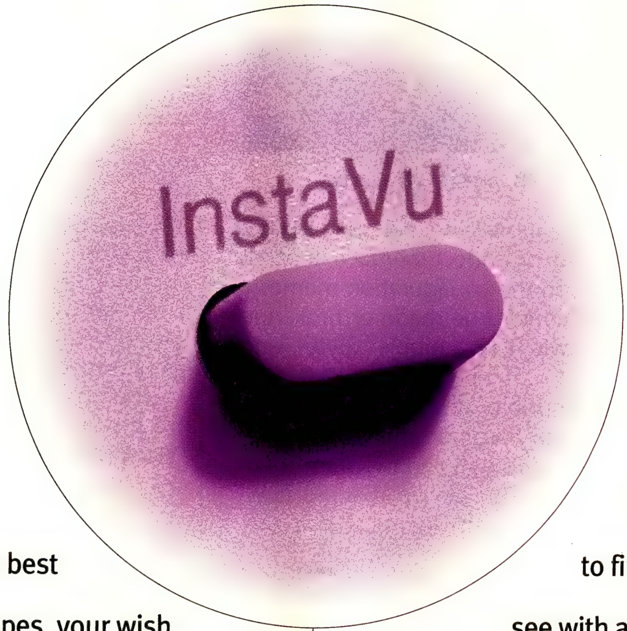

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CIRCLE NO. 214

Programmable switch features 2.4-Gbps bandwidth

I-Cube's new PS48, the first in a family of high-speed programmable switches, features 48 usable I/O ports, a 2.4-Gbps bandwidth, and a 100-MHz clock frequency. The PS products are designed for high-performance, high-bandwidth applications and suit the fast switching requirements of communications, image processing, and parallel processing. The switch connects via the RapidConnect interface, a parallel data bus that provides direct access to the configuration memory. RapidConnect allows buswide connections to be made or broken in 30 nsec or less. The PS devices can switch bit-, nibble-, byte-, and word-wide data paths.

The PS48 programmable switch provides 48 usable I/O ports.

The core of the PS device includes a nonblocking, enhanced-crossbar architecture, which features individually programmable I/O ports. Each I/O port is identical to the others, and you can program them as input, output, or bidirectional ports. The devices handle flow-through, clocked, and analog-signal flow with identical and predictable delays. The PS architecture also lets you connect ports one-to-one or one-to-many for applications that require multicasting of signals. Programmable crossbar-array connections let you configure I/O-port attributes from data stored in internal SRAM cells and registers.

The JTAG-compliant PS devices employ 0.8-μm CMOS technology. Future members of the family will include the PS96 with 96 usable I/O ports and the PS160 with 160 usable I/O ports. The PS48 is available now, and the 96 and 160 will be available in midyear. The PS48 costs $38 (1000).

—by John Gallant

I-Cube Inc, Santa Clara, CA. (408) 986-1077.

Circle No. 503

Chip directory lists 1100 companies and 14,000 contacts. The 1995 edition of Cypress Information Resources' *International Integrated Circuit Vendor, Product, and Contact Directory* is now available. The publication lists more than 1100 companies and organizations involved in manufacturing, designing, and licensing IC technology and products. The company-profile information includes main market segments, product lines, process technologies, product keywords, types of organizations, sales estimates, addresses, phone numbers, fax numbers, and contact names. The 610-pg directory costs $495 plus $15 for shipping and handling.

Cypress Information Resources, Los Gatos, CA, (408) 354-4887.

Circle No. 504

The Interface Group sells trade-show division. Conference and exposition producer The Interface Group has sold its trade-show division to Softbank Corp, Japan, for more than $800 million. The new name for the division will be SB Comdex when the transaction becomes final in mid-April. **The Interface Group**, Needham, MA, (617) 449-6600.

CALENDAR OF UPCOMING EVENTS . . .

June 21 to 23, 1995

Electro '95, Boston, highlights surface-mount technology and contract manufacturing. The IEEE, the Electrical Representatives Association, and the Institute for Interconnecting and Packaging Electronic Circuits are co-sponsoring the event. The conference includes surface-mount technology and manufacturing-services sessions that cover component standardization, ball-grid arrays, and flip-chip and chip-scale technologies. A surface-mount-technology production line will feature products and equipment from manufacturers. The program also will include more than 600 exhibitors and more than 100 product introductions. Miller Freeman Inc, Dallas, TX, (800) 223-7126.

Sept 28 to 29, 1995

Miniaturization '95, Singapore, features presentations of components, parts, and assemblies with emphasis on mobile computing, communications and electronics. Technical sessions will focus on low-power ICs, power management, physical and ergonomic miniaturization, and packaging and interconnect issues of electronic products. Workshops will feature the Personal Computer Memory Card International Association standard and ball-grid arrays. In addition, a session will cover these applications in products such as smart cards, laptops, and personal digital assistants. Contact: Julie Lim, Reed Exhibition Co, Singapore, (65) 371-0749.

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Huntsville, AL	**June 27**
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Irvine, CA	**June 21**
Kansas City, MO	**June 21**
Manchester, NH	**May 12**
Melville, NY	**June 6**
Milwaukee, WI	**May 11**
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Microchip PIC16/17 Microcontrollers

	DEVICE	PINS	I/O	MEMORY PROGRAM	MEMORY USER RAM
	PIC16C54A/CR54	18	12	512 x 12 (OTP/ROM)	25 x 8
	PIC16C55	28	20	512 x 12 (OTP)	24 x 8
	PIC16C56	18	12	1024 x 12 (OTP)	25 x 8
	PIC16C57/CR57A	28	20	2048 x 12 (OTP/ROM)	72 x 8
	PIC16C58A	18	12	2048 x 12 (OTP)	73 x 8
NEW!	PIC16C61	18	13	1024 x 14 (OTP)	36 x 8
NEW!	PIC16C622	18	13	2048 x 14 (OTP)	128 x 8
	PIC16C64	40/44	33	2048 x 14 (OTP)	128 x 8
NEW!	PIC16C65	40/44	33	4096 x 14 (OTP)	192 x 8
	PIC16C71(ADC)	18	13	1024 x 14 (OTP)	36 x 8
NEW!	PIC16C73(ADC)	28	22	4096 x 14 (OTP)	192 x 8
NEW!	PIC16C74(ADC)	40/44	33	4096 x 14 (OTP)	192 x 8
	PIC16C84	18	13	1024 x 14 (EEPROM)	36 x 8
	PIC17C42	40/44	33	2048 x 16 (OTP)	256 x 8

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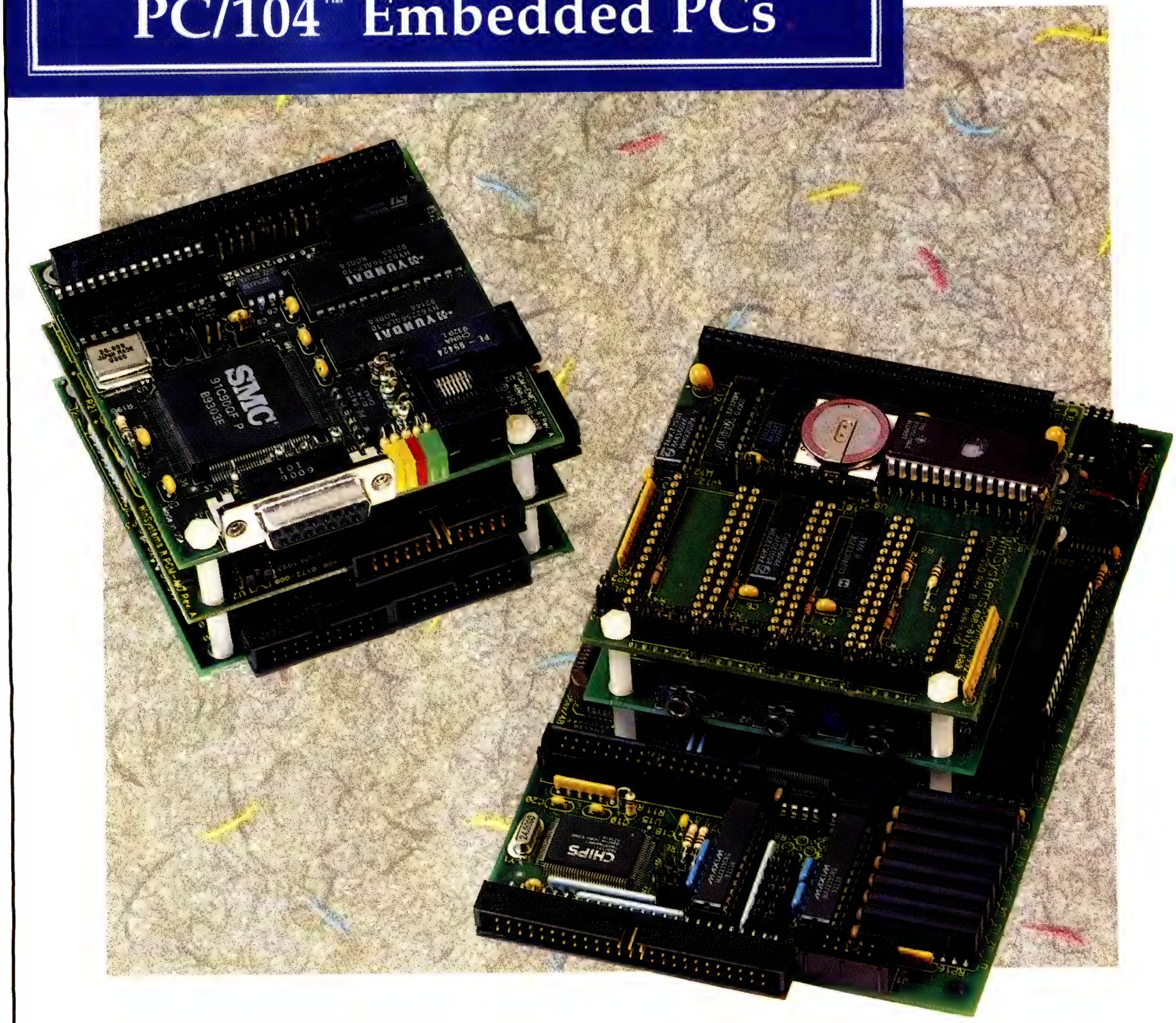

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Couch potatoes and convergence

"Convergence Reshapes Electronics" (*EDN* supplement, November 24, 1994), a report on the convergence of computers, communications, and entertainment television, was very well done, but it barely addresses one critical aspect: Will it sell?

I see only fleeting reference to consumers in Mr Young's article. Be wary of taking the word of focus groups. What consumers say they want might be quite different from what they will pay for in the cut-throat, discount retail marketplace. As good as the consumer survey might sound, the author quotes "experts" as recommending a 486 with SVGA monitor, some DSP, and a CD-ROM for low-end applications. What applications? It doesn't sound like anything I'd watch a Vikings game on.

When the average working stiff comes home, he or she grabs for the remote control, not a mouse. People want to push a button and see TV programs, not maneuver a mouse and chase icons. The last thing they will tolerate is having to fuss with a small screen such as a 14- or 19-in. VGA format, regardless of the increased resolution. The consumer's love of 40- to 60-in. projection-type NTSC receivers may cause consternation and hand-wringing among digital purists, but they had better learn to function in the real world—the analog one, that is.

In addition, consumers look at the price tag first and last, rarely buying more functionality than is absolutely necessary to do the basic job, which is to entertain. As a case in point, consider the fate of SVHS, touted to be the next wave of video recording, a forerunner of HDTV, which is now a dismal marketplace flop relegated to video-production studios. (We're still trying to unload some monitors we designed six years ago in anticipation of the consumer stampede that never occurred.) Was there a technical flaw with the SVHS system? Definitely not. The image is far superior to conventional VHS recording. What sandbagged SVHS was consumer apathy.

Here's an example why. About six years ago, I purchased a camcorder. My selections boiled down to two models, VHS or SVHS. Of course, the salesman pushed the superior image quality of SVHS to justify the higher price. My response was, "Great, I can play the tape back at home and have a better picture from my recorder."

His reply was, "No, you'll have to buy a new recorder."

I said, "Then I can play back with the new recorder and have a better picture on my TV?"

He responded, "No, you'll have to buy a new TV."

Needless to say, I bought the conventional VHS camcorder, and, as it appears, so has everyone else. I have the sinking feeling that HDTV might go the same route due to consumer apathy.

Wake up dreamers, you're dealing with coach potatoes, not movie producers or computer hackers. The masses expect to be entertained, on cue.

The computer and the TV are going to be much like the toaster and the oven, each doing its job similarly but separately. Somewhere in between, for those who cannot decide which to buy, will be the video-equipped PC that, much like the toaster oven, is a good idea that is not about to replace either the toaster or the oven. I've spent most of my career in the display industry, working in broadcast television before moving into video-monitor design. The TV viewer is fickle and, for the most part, a computer-wary consumer, avoiding overly complicated equipment whenever possible.

I predict that the company that goes overboard to pursue the fantasy of a family clustered around a PC for an evening of TV viewing is going to be rudely surprised in the marketplace. Send one of your reporters down to the local Wal-Mart to find out what people are actually buying. We may just discover different, more accurate trends than the so-called experts and focus groups offer.

David G Storberg,
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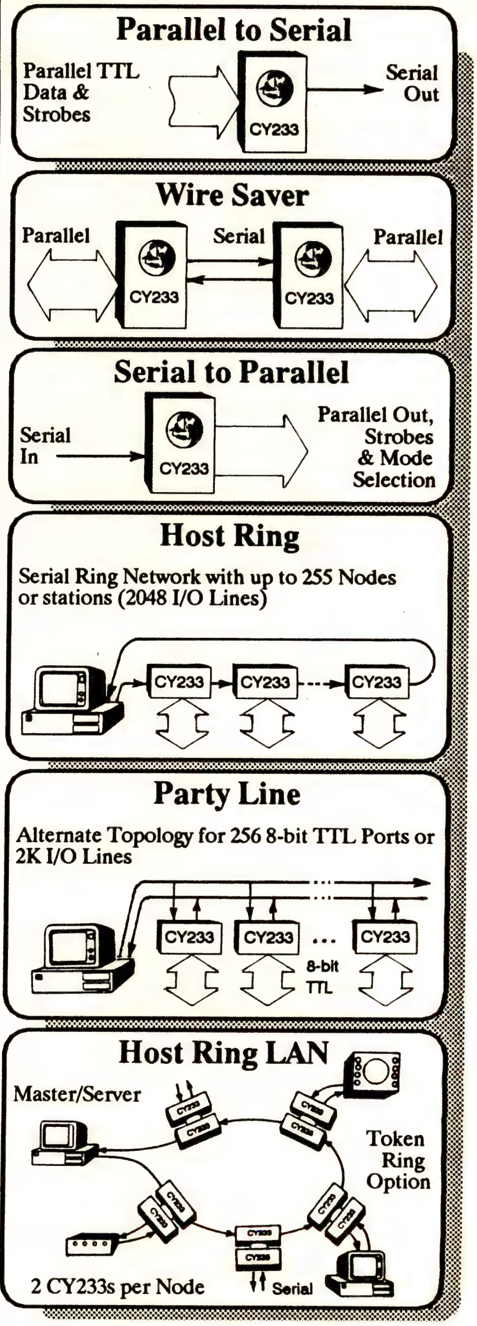

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On the shoulders of giants

When we contemplate powerful desktop computers, multimillion-transistor digital ICs, and op amps with practically infinite gain and no offset, we tend to think of the geniuses who made such wonders possible. In information theory, great thinkers such as Von Neumann and Wiener come to mind. In ICs (and semiconductors, in general), we think of Shockley, Bardeen, and Brattain at Bell Labs; and Kilby and Noyce. In linear technology, we have Dobkin, Philbrick, Redfern, and Widlar. Continuing the tradition of honoring such innovators, this issue's "Out in Front" section features the winners of this year's "Innovator and Innovation of the Year Awards."

What we perhaps forget is that these great innovators had a lot of help from the giants who preceded them by decades or even centuries. The striking characteristic of the early inventors is that their ground-breaking work was theoretical and certainly not aimed at producing a salable product. What they produced was pure knowledge. The gifts they gave us in mathematics, physics, and logic made it possible for the practical innovators to produce their marvels.

> **Great innovators get a lot of help from the giants who preceded them.**

Consider the great mathematicians of centuries ago. Leibnitz and Newton, for example, did not co-develop the calculus to build better bridges or to analyze circuits. And, in their work with equations, complex algebra and calculus, and general numbers theory, the great mathematicians Cardan, Cauchy, Euler, Fourier, Gauss, and Laplace had no idea their pioneering theories would prove so essential to 20th-century technology.

Let's take the examples of complex math and Laplace. Complex math, using an outlandish, nonexistent quantity called an "imaginary number," makes it easy for us to analyze reactive circuits. A 19th-century mathematician, just for the theory of it, found that multiplying by $\sqrt{-1}$ is equivalent to rotating a vector on a graph by 90°. What a lucky coincidence—we can use "j" for reactive impedances, and the circuit-analysis math becomes easy. The same holds true for Laplace and his "s" operator and transforms. Laplace developed his theories for the pure math of it, with no practical applications in mind. Luckily, his findings let us easily determine the stability of second-order systems.

The computer I'm writing with uses binary logic and arithmetic. Several generations of software developers have made it possible for me to click on a mouse and discard a file into a trash-can icon. What's easy to forget is that computing owes a lot to the geniuses of previous centuries. Leibnitz, for example, was fascinated by binary arithmetic and developed many applicable principles. But, it was Boole in the 19th century who poured the foundation for binary logic. He developed an entire mathematics of symbolic logic—just for the theory of it. AND, OR, NOR, and exclusive OR all come from the great logician Boole. Other early geniuses, such as DeMorgan and Karnaugh, further refined Boole's binary math.

I'm not all that familiar with the history of physics, but I'm sure our contemporary semiconductor-process physicists owe a great debt to their predecessors in pure atomic, diffusion, and field theory. I recall reading that, by the 1920s, the theoretical basis for making an FET was already in place. It took technology about 40 years to catch up to the theory.

In the wonderful process called "progress," each innovator, whether theoretician or technologist, stands on the shoulders of giants. It's true not only in electronics, but also in physics, biotechnology, aeronautics.... For example, Oppenheimer, Szilard, and Teller, among many others, could not have done their towering work in the Manhattan Project without recourse to the theoretical groundwork of Bohr, the Curies, and Rutherford. And these early theoretical geniuses never stopped to ask themselves, "What's the practical application of this?"

We tend to look upon innovation as a creative tool to produce something practical. That's not always the case—there's room for blue-sky thinkers whose work doesn't seem to be of any immediate application. Maybe 40 years from now, some current ideas with no immediate practical applications will spawn entire new technologies and industries.

Bill Travis

BILL TRAVIS
SENIOR TECHNICAL EDITOR

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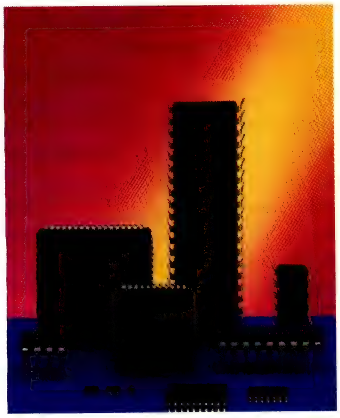

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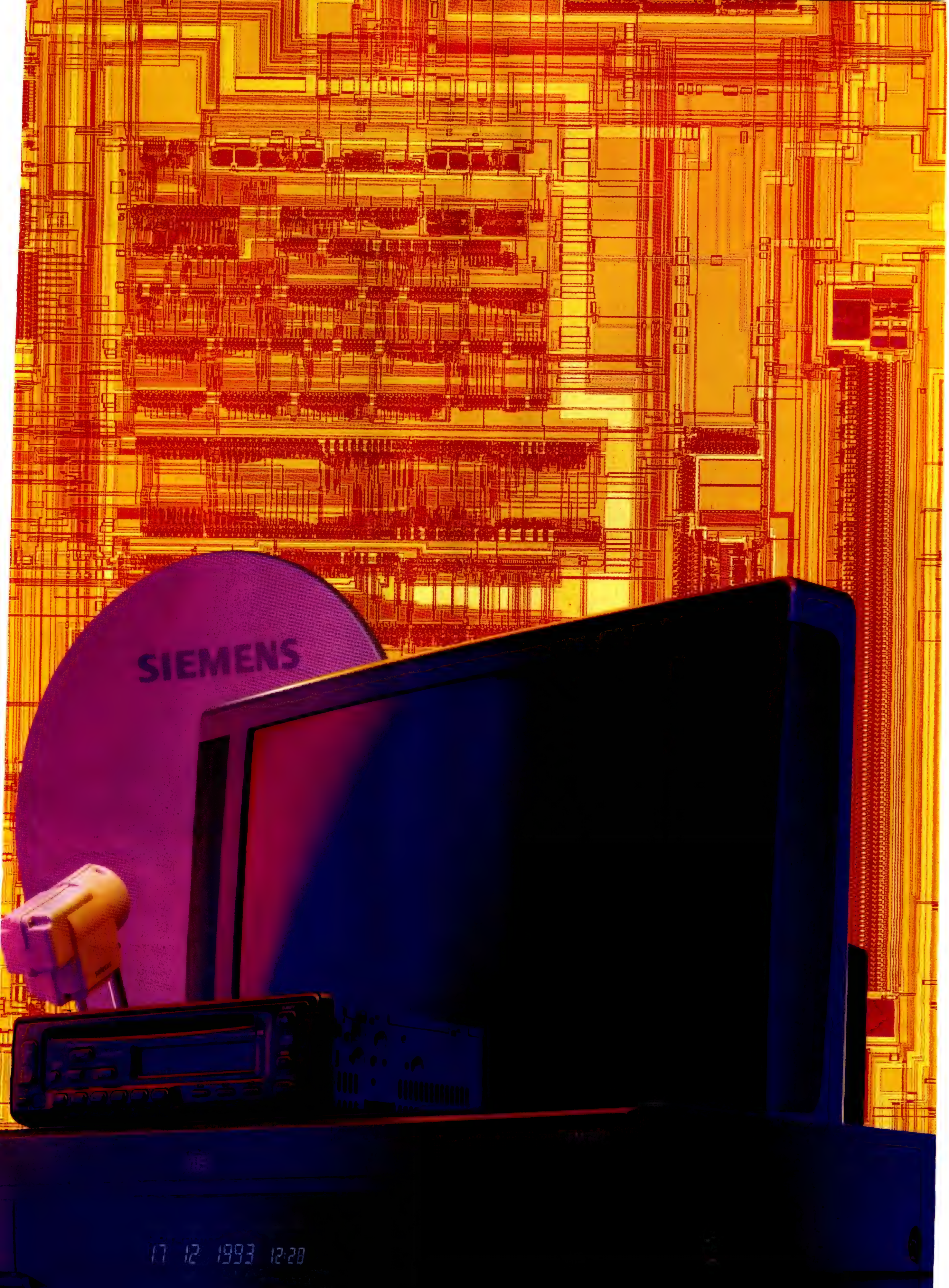
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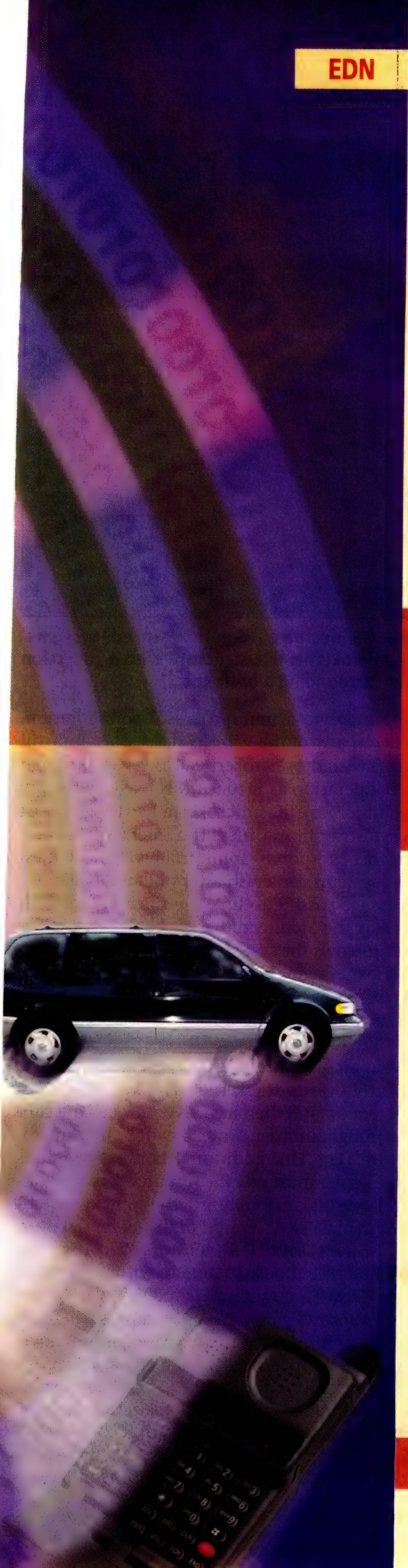


Microkernel and modular OSs

RICHARD A QUINNELL, TECHNICAL EDITOR

To produce more compact and adaptable code, software vendors are segmenting their operating-system kernels into modules surrounding a microkernel. As a result, they can offer a standard OS with custom configurability using minimal memory resources.

Operating systems (OSs), large and small, are evolving. Monolithic structures are giving way to modular designs. The OSs' modularity, in turn, allows designers to readily adapt them to new environments, prune off and graft on needed services, and plant commercial OSs into application niches in which they could never before thrive.

A growing adoption of microkernel architectures is driving this OS evolution. **Ref 1** defines a "microkernel" as a program that provides four minimal services:

- Interprocess communications,
- Low-level input and output capability,
- Limited scheduling and process management, and
- Basic memory management.

All other traditional OS services, such as file and directory management, reside as user-level servers outside the microkernel.

The microkernel architecture debuted in Unix OSs. Unix developers had, over time, added many functions to their monolithic kernels. The ultimate results were multimegabyte OS kernels. To make those kernels smaller, the designers of OSs such as Chorus Systems' Chorus Nucleus, the Open Software Foundation's Mach 3.0, and QNX Software Systems' QNX turned to

Photograph courtesy Microtec Research

MICROKERNEL AND SCALABLE OSs

the microkernel architecture. Designers reduced the kernel to the bare minimum—10 to 100 kbytes. The term "microkernel" reflects the system's size relative to the monolithic original.

The microkernel architecture, a bare-bones core with a collection of serverlike system-resource providers, is inherently modular. This modularity, in turn, provides the microkernel OS with tremendous advantages over monolithic designs. These advantages include simplified maintenance and modification, portability to new processors, flexible operation, an ability to run while distributed over multiple processors, and compact code.

The microkernel approach's modular nature simplifies the problems of code maintenance and modification. In contrast, many traditional monolithic OSs grew without structure, as designers repeatedly added code over years. As a result, monolithic designs developed internal coupling, allowing modifications in one section to affect the operation of other—apparently unrelated—sections. Thus, designers must take care when attempting to fix bugs or extend a monolithic OS's capability, making maintenance and modification difficult. End users who modify a commercial OS to meet their needs do so at some risk.

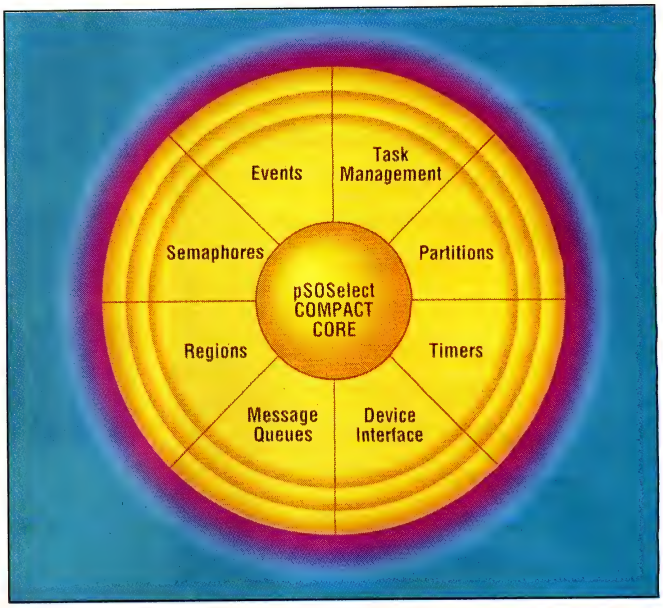
With the microkernel approach, designers can add and debug new system-service modules with less risk of system crashes because these services run in protected memory at the user level. Errors within the modules do not affect the OS kernel, and adding a service does not introduce conflicts with existing services. The microkernel approach also allows service-module designers to employ the range of debugging tools available to application designers. The system servers are, after all, running at the user level, just as an application program does.

Microkernel designs can simplify porting an OS to new processors. The microkernel encapsulates most of the processor-dependent software in a small, manageable package. Once a designer ports the microkernel to the new processor, the designer can simply recompile the remainder of the OS, rewriting only those services that the new processor does not physically support.

Flexibility is another hallmark of a microkernel OS. A microkernel system's personality traits, such as file formats and user interfaces, reside in servers. The user needs only an appropriate set of servers to obtain any OS personality. In addition, the OS can support more than one personality. If the OS contains a collection of servers for different personalities, the system can appear as a Unix machine for one user, a DOS machine for another, and so on. Further, the microkernel OS allows dynamic modification. You can add or delete system resources while the system remains running; you need not reboot. This feature makes the microkernel OS perform the software equivalent of hot-swapping boards.

Message-passing=multiprocessing

The system-resource servers that compose the OS interact with the microkernel by exchanging messages. The messages need not pass through registers or shared memory; they can just as effectively move over a network. A microkernel OS, therefore, readily maps to a multiprocessor configuration. Servers can reside on any of the various processors and still exchange messages with the microkernel. However, although such distributed operation is structurally easy with any microkernel architecture, the microkernel's design must incorporate such distribution. Unless the interprocess communications protocol responds appropriately to lost messages, distributed systems can crash after one node fails.



Many real-time OS designs, like Integrated Systems' pSOSelect, use a microkernel-like structure with a collection of system servers surrounding a basic core.

The use of message-passing to link the microkernel with the rest of the OS is the architecture's major drawback (**Fig 1**). The architecture slows the system down. Part of the slowdown occurs as the messages propagate. The rest of the slowdown comes as a result of context-switching between microkernel and servers when the application calls upon an OS resource.

In a monolithic architecture (**Fig 1a**), a context switch turns system control over to the kernel. The kernel services the application's request and then returns control to the calling application through another context switch. In a microkernel architecture (**Fig 1b**), additional context switches occur because the kernel must call the resource server to satisfy the request. The result is a doubling of the context-switching overhead of system calls. As a result of this potential overhead penalty, some Unix OS vendors serving the embedded-system market choose to remain with monolithic architectures. Lynx Real Time Systems' LynxOS, JMI Software Systems' PSX, and VenturCom's Venix, for example, all operate as integrated, monolithic OSs to achieve top performance.

The magnitude of the overhead penalty is a subject of much debate in the Unix community. Some researchers claim that the performance can degrade as much as 15%. Others claim that the penalty is insignificant if the context-switching and message-passing time is substantially shorter than the service requires. Still others find that the microker-

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MICROKERNEL AND SCALABLE OSs

nel's modularity allows them effectively to fine-tune service routines and show an overall performance improvement of 10%. Lacking consistent results, the microkernel-overhead-penalty debate has become a religious, rather than scientific, argument.

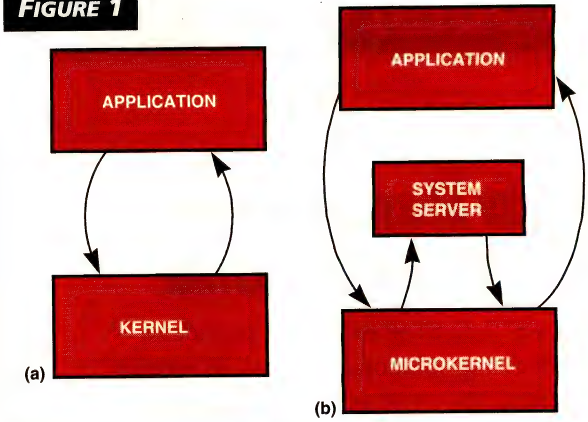
The penalty notwithstanding, vendors of non-Unix real-time OSs for embedded applications have embraced—although not fully—the microkernel concept. To avoid the penalty, most real-time vendors stopped short of a full microkernel architecture in new designs. Instead, vendors have built scalable OSs using a microkernel-like collection of independent functional modules surrounding a core of basic services.

The vendors' marketing literature sometimes refers to core services as a "nanokernel" and to the entire OS as a "microkernel." The assembled OS, however, is still monolithic, in that OS services run in supervisor mode along with the kernel. Nonetheless, by building the OS from modules rather than as an integrated whole, vendors inherit the microkernel approach's scalability and can offer extremely compact code.

At first glance, a modular design would seem most likely to result in larger, not smaller, code. The OS would need additional code, for example, to handle message-passing. Also, independent modules might duplicate some functions. A glance, however, doesn't encompass the entire picture. Further examination shows that modularity can help save code. The designers of Microware's Atomic OS-9, for example, found that modularity allowed them to optimize their code more fully. Because the modules were independent, the designers could tune modules without complicating another function. The result is a 15% size decrease.

Modularity also yields compact code because it lets end users assemble only the minimum set of OS functions their projects require. Trimming the fat from commercial OSs isn't practical with monolithic designs; it's too risky. Integrated monolithic designs, therefore, leave designers with an all-or-nothing choice. A microkernel-like OS, on the other hand, lets a user scale the OS's overall size to better fit a system's memory resources.

FIGURE 1



The major drawback of a microkernel design is additional context-switching overhead. A monolithic OS (a) has one pair of context switches for a system call. A microkernel OS (b) has two pairs because the system service lies outside the kernel.

This scalability is allowing microkernel-like OSs to become viable commercial alternatives to custom OSs in deeply embedded applications. Such applications need both OS and application programs to reside entirely within a microcontroller's on-chip ROM. Commercial-OS vendors are achieving this goal. Microtec Research's VRTXmc, for example, can produce a basic kernel that occupies approximately 4 kbytes of ROM. The Integrated Systems pSOSelect scales down to 1800 bytes.

The main difference between scalable OSs and true microkernels is that scalable OSs are still monolithic. Once you assemble the OS, you cannot add or delete system functions to or from the OS using programs in user space. Instead, you

LOOKING AHEAD

Whether to a true microkernel or to a microkernel-like design, integrated monolithic operating systems (OSs) are evolving—from single-celled organisms to creatures comprising a collection of specialized cells. With this evolution come new capabilities for the OS. The evolution also may bring a new paradigm to the production and sale of commercial OSs.

The distinctions between OSs increasingly result only from differences in their microkernels. Those distinctions will become less significant as more vendors embrace the microkernel approach. The microkernel moves the system's personality into a user's space where the user can modify that personality. The next logical step is for the market to gravitate toward a select few microkernels. Alternatively, vendors may take control of their destiny and agree to standardize on a microkernel or at least the service interface for a microkernel. Either way, more systems will build on the same core software.

With many systems built upon a common core, a new category of software—middleware—will emerge, thus, opening a market for suppliers of system-service modules that work with the common core. OS software will become like a processor and its peripherals in that you simply hook them together to make what you need. The key is to standardize on the base microkernel so that there are enough standard-base systems to support a middleware market.

Vendors are already jockeying to establish the winning microkernel. Chorus Systems is promoting its Nucleus as an open microkernel standard. Digital Equipment Corp and IBM are also in the running. The two have teamed to develop and promote an open microkernel based on the Mach technology. Other companies are likely to join the race, as well. Who will emerge as the winner is anyone's guess.

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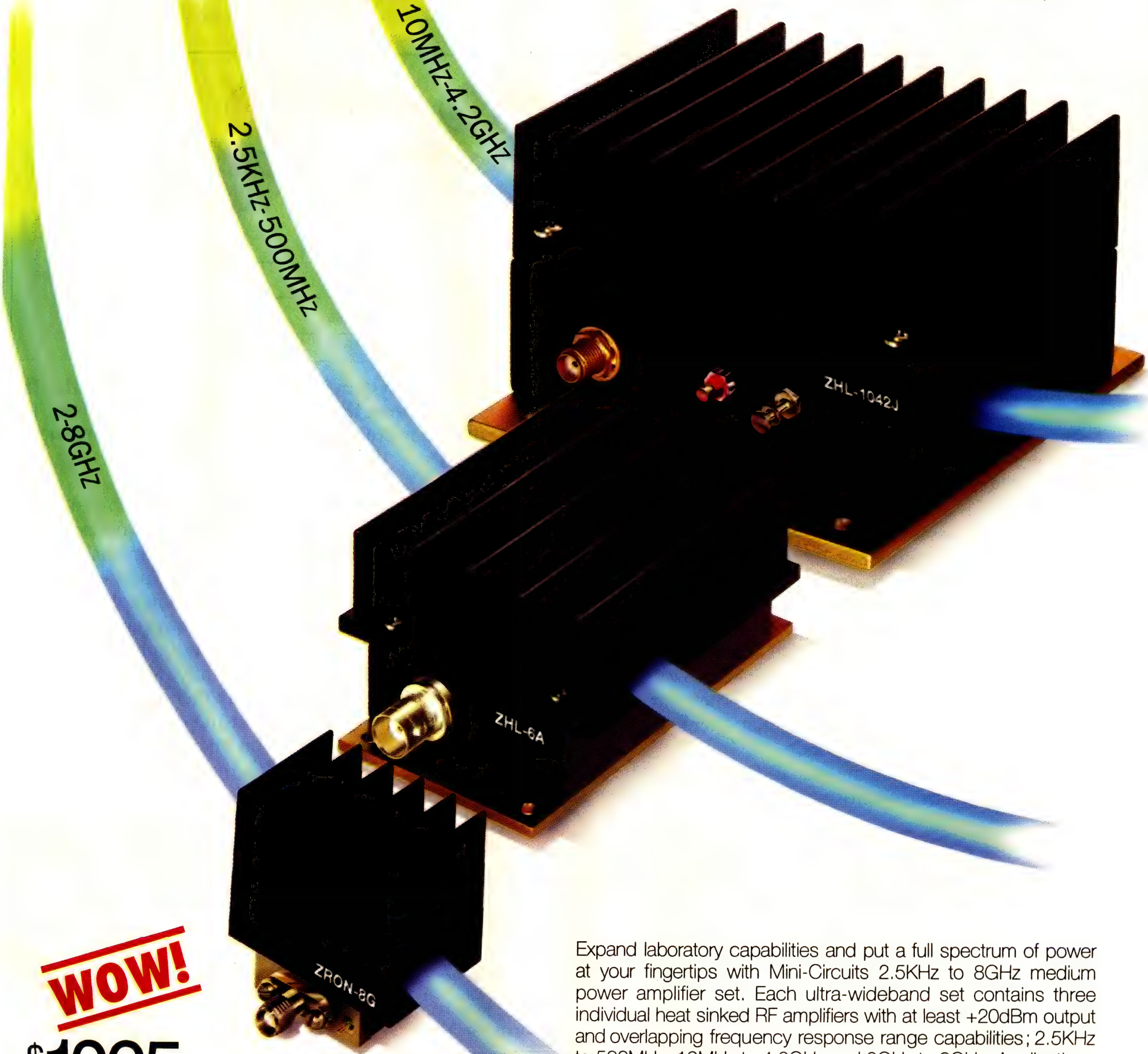

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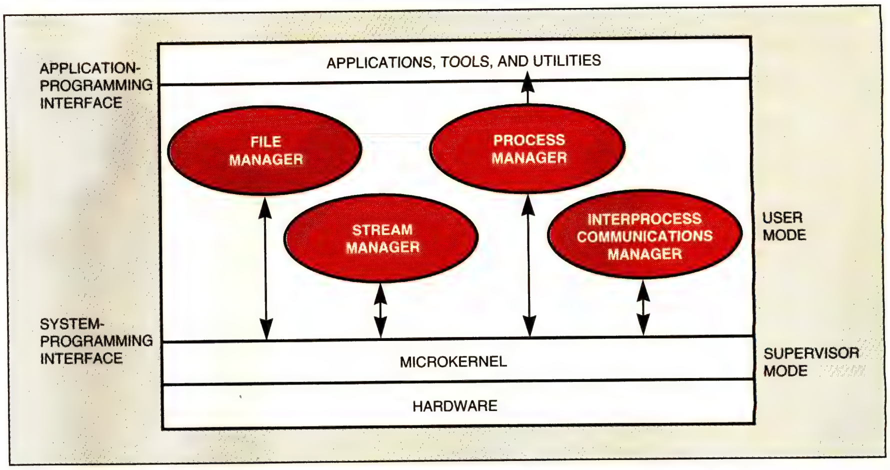
must reassemble the OS whenever you make a change. The modular approach still simplifies the task of adding unique functions to the OS kernel, however, because the new module is relatively independent of the others. The modules no longer have memory protection, however, because they all operate in the supervisor mode. Thus, design errors in the new module can crash your system.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The microkernel architecture puts the system functions into servers, separating the application-programming interface from the system-programming interface. The additional interface layer allows a microkernel to mimic other OSs by managing the application interface.

Modularity methods vary

Vendors of real-time OSs differ in their approaches to leveraging the modularity inherent in their new OS designs. For example, Microtec Research offers two options. It created VRTXmc, which allows you to select from more than 33 services to build a monolithic OS. The services are so fundamental that the OS requires no core nanokernel. You simultaneously assemble both the equivalent of the nanokernel and the remainder of the OS. For more substantial needs, Microtec Research also offers VRTXsa, a true microkernel with modular-OS services.

Integrated Systems offers a single user-scalable OS, pSOSelect, a scalable version of the pSOS+ OS that is fully upward-compatible with its parent. Projects that outgrow the scalable version can readily migrate to pSOS+. The company also offers a version of pSOS, pSOS+m, that operates while distributed over multiple processors.

Rather than offer users the mix-and-match capability of a scalable OS, Spectron Microsystems offers its SPOX DSP OS as a product family. The family members are all based on the same SPOX nanokernel but offer combinations of services for various applications. Because the family members are standard products, not users' own kit productions, users don't have to debug the OS. The family's common core makes the products compatible with each other, however, so designers need not learn a new OS with each new application.

Microware also offers a product family, which is based on its Atomic OS-9 kernel. Each family member builds on the one before by adding utilities and I/O capability. The base version is small enough to fit into microcontrollers, and the high-end member of the family is the full-scale workstation-based OS-9, Version 3.0.

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MICROKERNEL AND SCALABLE OSs

One drawback that application developers face when using scalable OSs is that paring the OS may cut links to debugging tools. Many RTOS vendors put "hooks" in their kernels that enable debugging tools to provide information on the timeliness and logical flow of code execution (**Ref 2**). The nanokernels of scalable OSs lack these hooks. Thus, if you want to keep the OS small, you may lose the ability to monitor the code's execution. In such cases, you must turn to hardware-based debugging tools to trace code execution. ROM emulators are one such tool, and, if your processor supports on-chip debugging, you have other options (**Ref 3**).

Another possibility is to debug your code on a memory-augmented version of your final product using more than a bare-bones OS. When it comes time for production, you can then scale the OS to fit your normal memory limits. Spectron Microsystems' SPOX, for example, offers a debugging module that you can remove from the OS for production.

Even though the scalable-OS approach may limit tool selection, commercial OSs offer a broader tool selection than homemade designs. If you're used to creating custom OSs for embedded projects, then you might reconsider purchasing an OS to gain tool support. The commercial OS gives you the freedom to focus on your application without first becoming an OS expert. Purchasing a microkernel or modular OS also provides some assurance that you'll have ready access to future innovations in OS design—just add modules. EDN

References

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You can reach Technical Editor Richard A Quinnell at (408) 685-8028; fax (408) 685-8028.*

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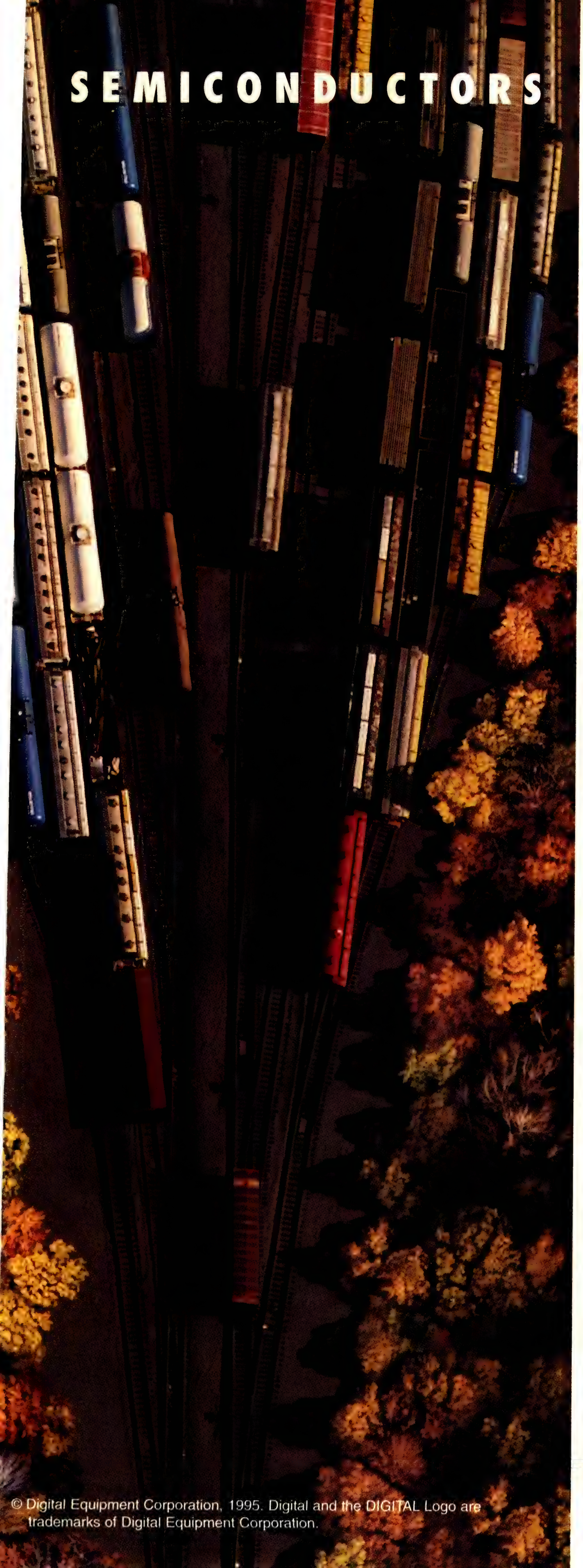

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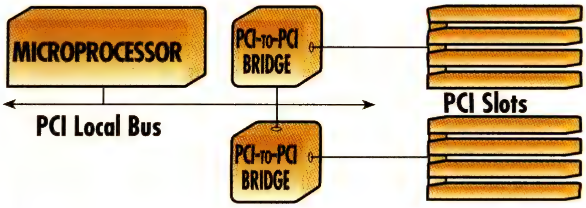

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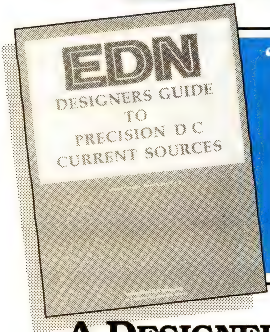

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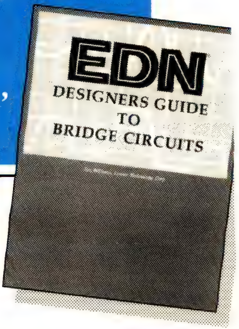

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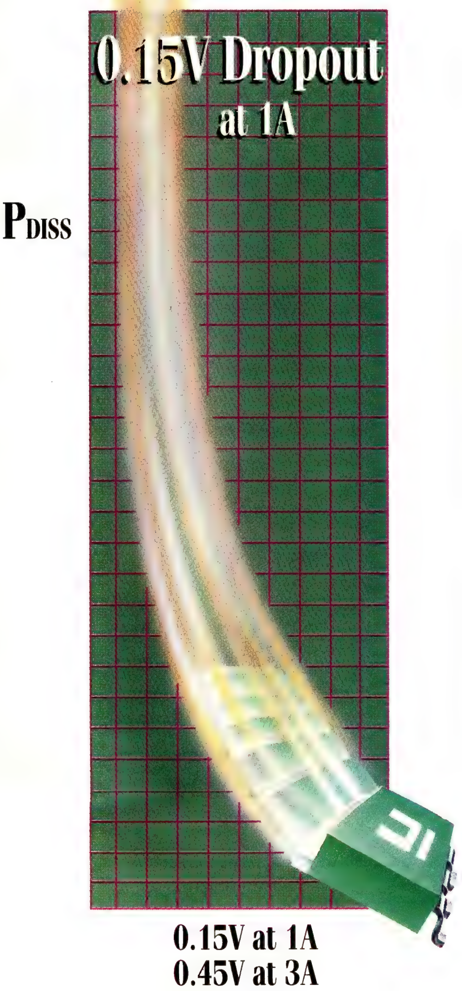

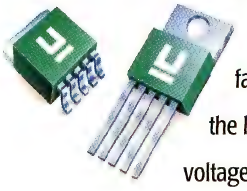

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SNEAK PREVIEW:

Products from the Embedded Systems Conference

Microprocessors, single-board computers, development tools, in-circuit emulators, compilers, debugging tools, and microcontrollers—these are just some of the products that will be introduced or displayed at the Embedded Systems Conference. The show will be held April 18 to 20 at the Inforum in Atlanta, and will include exhibits of products and a choice of more than 60 lectures on the different aspects of working with embedded systems.

For a preview of the show's products, see the highlights below. For more information on the conference, phone (415) 905-2354.

Development tool for interactive real-time graphical applications under Unix and Windows. The VAPS tool sets helps you build real-time graphical human-to-machine interfaces. The suite includes entry-level prototyping through advanced applications running on multiple platforms. VAPS/Prototyper ($9500) is an entry-level tool for human-factor specialists and designers whose need to prototype real-time interactive graphical applications. VAPS/Designer ($16,500) suits advanced, real-time, interactive, graphical prototypes. VAPS/Developer ($34,500) generates C code for working beyond the prototyping phase. VAPS/Rehost ($41,500) is a complete development tool from prototyping through deployment on multiple target platforms. The VAPS/C-Code Generator ($10,000 for Windows) lets you create an application under Unix and then generate C code for the application to run under Windows on PCs. The tool confines development, debugging, and maintenance to just the Unix version, simplifying development. The C-code generator for Windows costs $10,000. **Virtual Prototypes Inc**, Montreal, PQ, Canada. (514) 341-3874.

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EMBEDDED SYSTEMS PRODUCTS

Real-time kernels for Motorola IDP board with 68060 processor have 2-μsec context switch. The ROMable C Executive multitasking operating-system kernel has 14 of its 56 system calls identical to those of Unix. The PSX real-time kernel adds 55 Posix.1 system calls to the basic C Executive kernel. Systems calls are an execute-only subset of the system calls normally on Unix workstations. The initial copy of C executive costs $2500, dropping to $20 (1000). The initial copy of PSX costs $3750, dropping to $30 (1000). **JMI Software Systems Inc**, Spring House, PA. (215) 628-0840. **Circle No. 466**

Modular ICE for 68300 microcontrollers lets you tailor price/performance. The Vision/Control base system ($3150) includes a target controller for the VisionICE in-circuit emulator (ICE). Vision/Control configures and coordinates the operation of all other hardware and software modules and can function as a stand-alone, background-debugging-mode emulator. It includes a hardware diagnostic executive, a flash-memory-programming interface, and a high-speed parallel download. The Vision/Event module ($4600) provides 64 hardware comparators, which you can combine and nest up to eight levels deep. You can use the event outputs to break execution or to trigger a fully selectable 64,000-frame×144-bit, real-time trace buffer. You can view this trace buffer while the target system continues to run in real time. The Vision/Net card ($2450) adds Ethernet-network capability, and the Vision/Mem module ($1000) provides up to 1 Mbyte of overall emulation memory. **Embedded Support Tools Corp**, Canton, MA. (617) 828-5588. **Circle No. 467**

40-MHz microcontroller delivers zero-wait-state performance from 70-nsec memory. The AM188EM microcontroller provides the address externally a half-cycle early, eliminating the need for external address latching. The microcontroller provides an 8-bit data bus, synchronous and asynchronous serial ports, and 32 bidirectional, programmable I/Os. The device also includes a 16-bit reset-configuration latch, six external and seven internal interrupt channels, an enhanced chip-select function offering up to 15 wait states, and a programmable clock driver. The chip is available in 10-, 25-, 33-, and 40-MHz versions in TQFPs and PQFPs. From $8 (10,000). **Advanced Micro Devices Inc**, Austin, TX. (512) 602-5651. **Circle No. 468**

68HC16 development kit supports C-language development. The 68HC16 development kit includes an ANSI-compatible C cross-compiler. The software supports the address space of the device and uses the multiply-accumulate and DSP features of the device. It allows near, far, and huge pointers to functions or data, providing different memory models for data sizes from 64 kbytes to 1 Mbyte. The development kit also includes a structured assembler that includes a C preprocessor, allowing full use of ANSI C macros, conditional statements, and C-include files within the assembler. Other features include a linker, a high-level simulator/debugger with full symbolic and C source-level simulation, and a built-in assembler/disassembler for manipulation of code during runtime debugging sessions. $1495. **IAR Systems Software Inc**, San Francisco, CA. (415) 765-5500. **Circle No. 469**

Real-time OS for PowerPC offers improved read/write performance. LynxOS version 2.3 offers a file system that provides faster read and write performance than the 2.2.1 release. The new version also offers an improved Gnu's Not Unix (GNU) development tool chain and updates all compilation tools, including GDB, GCC, G++, and Make, to the 2.6 Cygnus-Standard release. The new version is ANSI-compliant and supports graphics-card, Peripheral Component Interconnect, enhanced Ethernet, SCSI, and enhanced integrated-device-electronics cards. Prices range from $3000 to $6000. **Lynx Real-Time Systems Inc**, Los Gatos, CA. (408) 354-7770. **Circle No. 470**

Prototyping platforms for 32- and 64-bit RISC and CISC systems let you evaluate CPUs. The Cogent Modular Architecture (CMA) prototyping platforms let you interchange CPU modules from major IC vendors to evaluate performance with different CPUs. Available processors include the Advanced Micro Devices 29000; the IBM PowerPC; Integrated Device Technology MIPS; Intel i960; the Motorola 68000, 683XX, and PowerPC. The system connects to a Sun or PC host via a serial port or Ethernet and works with the complete Gnu's Not Unix (GNU) C/C++ tool chain. Base systems start at $1995, and CPU modules start at $795. **Cogent Computer Systems Inc**, Marlborough, MA. (508) 624-6447. **Circle No. 471**

Eight-slot PCI system board with i960 RISC processor targets embedded-system applications. The SB08 has Peripheral Component Interconnect (PCI) slots that let you use industry-standard PCI I/O cards for fast and inexpensive development. The system board uses sectored, in-circuit-programmable flash ROM for downloading application code. Initialization and PCI BIOS routines reside in write-protected sectors. The board uses two local-bus-to-PCI bridge devices supporting peak transfer rates to 132 Mbytes/sec. DRAM capacity ranges from 2 to 128 Mbytes in standard 72-pin SIMM sockets. The company offers real-time-development environments for the board from Inte-

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grated Systems and Wind River Systems. The SB08-JF33-102 costs $968 (1000). **Cyclone Microsystems**, New Haven, CT. (203) 786-5536.
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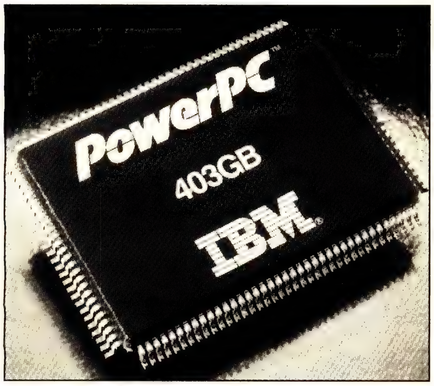

Embedded controller integrates peripheral functions and offers 61,000-dhrystone/sec performance. The PowerPC 403GB, a 32-bit 28-MHz microcontroller, targets printers, scanners, set-top boxes, and X-terminal applications. The controller integrates a two-channel DMA controller, a DRAM controller, an I/O controller, two-way set-associative instruction and data caches, a multilevel interrupt controller, multiple timers, and a flexible bus interface to allow direct attachment of memory and peripherals. Power consumption is 200 mW at 28 MHz. The device comes in a 28-pin PQFP and costs $45 (1000). The 33-MHz PowerPC 403GA is also available and costs $53 (1000). A 25-MHz version of the 403GA costs $49 (1000). **IBM Microelectronics**, Hopewell Junction, NY. (800) 769-3772.
Circle No. 473

Real-time debugger hardware for 80386 and 80486 processor-based systems. Embedded Periscope is a line of real-time debugger-hardware products for embedded-software developers. The product provides capabilities similar to those of in-circuit emulators at a cost of $3000 to $4000, depending on the target environment. The initial offering will include compatibility with Phar Lap and Soft-Scope software tools. **The Periscope Co Inc**, Atlanta, GA. (404) 888-5335.
Circle No. 474

JTAG emulation for the PowerPC links cross-development activities. The NetROM JTAG product provides a communication path between the target system being debugged and the host development station. Communication with the target system is through the target's ROM socket or UART. Communication with the host system is via Ethernet, eliminating the need for Ethernet hardware or software on the target system. You can nonintrusively single-step code, set breakpoints, and run memory tests and other functions. The tool's ROM-emulation capability lets you download up to 1 Mbyte of code in 18 sec. $5595. **Xlnt Designs Inc**, San Diego, CA. (619) 487-9320.
Circle No. 475

C++ development tools for 680x0 μPs. This tool set includes the Xray debugger, a C++ compiler, an assembler, a linker, and the Xray MasterWorks productivity tools. According to the company, the C++ compiler suits embedded-software development and conforms to the Annotated Reference Manual standards. New features of the compiler included templates to simplify reuse of source code and exception handling that provides efficient recovery from synchronous errors. The compiler directly compiles C++ source code into object code, resulting in fast compilation. From $4250. **Microtec Research Inc**, Santa Clara, CA. (408) 980-1300.
Circle No. 476

16-Mbit flash memory mimics the operation of a standard disk drive. The NM29M16 suits use in embedded applications. It operates from a single 5V supply and comes in a 44-pin TSOP. $52 (1000). **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959.
Circle No. 477

SCSI-2 board for VMEbus supports a variety of real-time operating systems. The PT-VME432 works with HP-UP, SunOS, Solaris, Microware OS/9, and Wind River VxWorks. The board provides VME 64 and SCSI-2 compatibility, making it possible to move data at a sustained rate of 17 to 19 Mbytes/sec. It accommodates as many as 30 SCSI-2 devices. From $2195. **Performance Computer**, Rochester, NY. (716) 256-0200.
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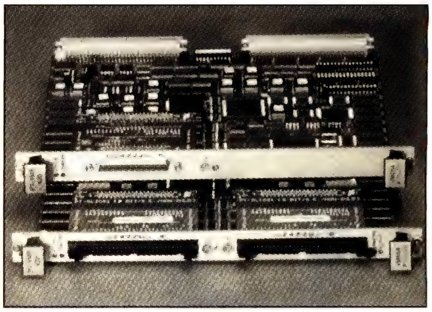

Real-time operating system supports a wide variety of 8-, 16-, and 32-bit processors. RTXC V3.2, a multitasking, real-time executive, provides a ROMable and configurable operating system. The operating system supports a range of CISC, RISC, and DSP microcontrollers and μPs, including the Hitachi H8/5xx, the IBM PowerPC, the Intel 80x86, the Motorola 68xxx and MC68HC11/16, the NEC V20/25/53, the Siemens 80C165/166/167, the Texas Instruments TMS320C3x, and the Zilog Z80/Z180. The company distributes the royalty-free real-time operating system in ANSI C source code. It provides over 70 kernel services in task management, semaphore services, queue services, mailbox and message services, memory management, and timer management. From $1495. **Embedded Systems Products Inc**, Houston, TX. (713) 728-9688.
Circle No. 479

Alpha AXP-based single-board computer has VME and PCI local-bus interfaces. The VMEAlpha64/XP single-board computer is based on the 275-MHz 21064 Alpha AXP RISC processor and provides peak execution of 550 MIPS. The two-board, 6U module incorporates an optional i960 RISC I/O coprocessor, D64 transaction support, configurable cache and memory, Peripheral Component Interconnect (PCI) bus for high-performance Ether-

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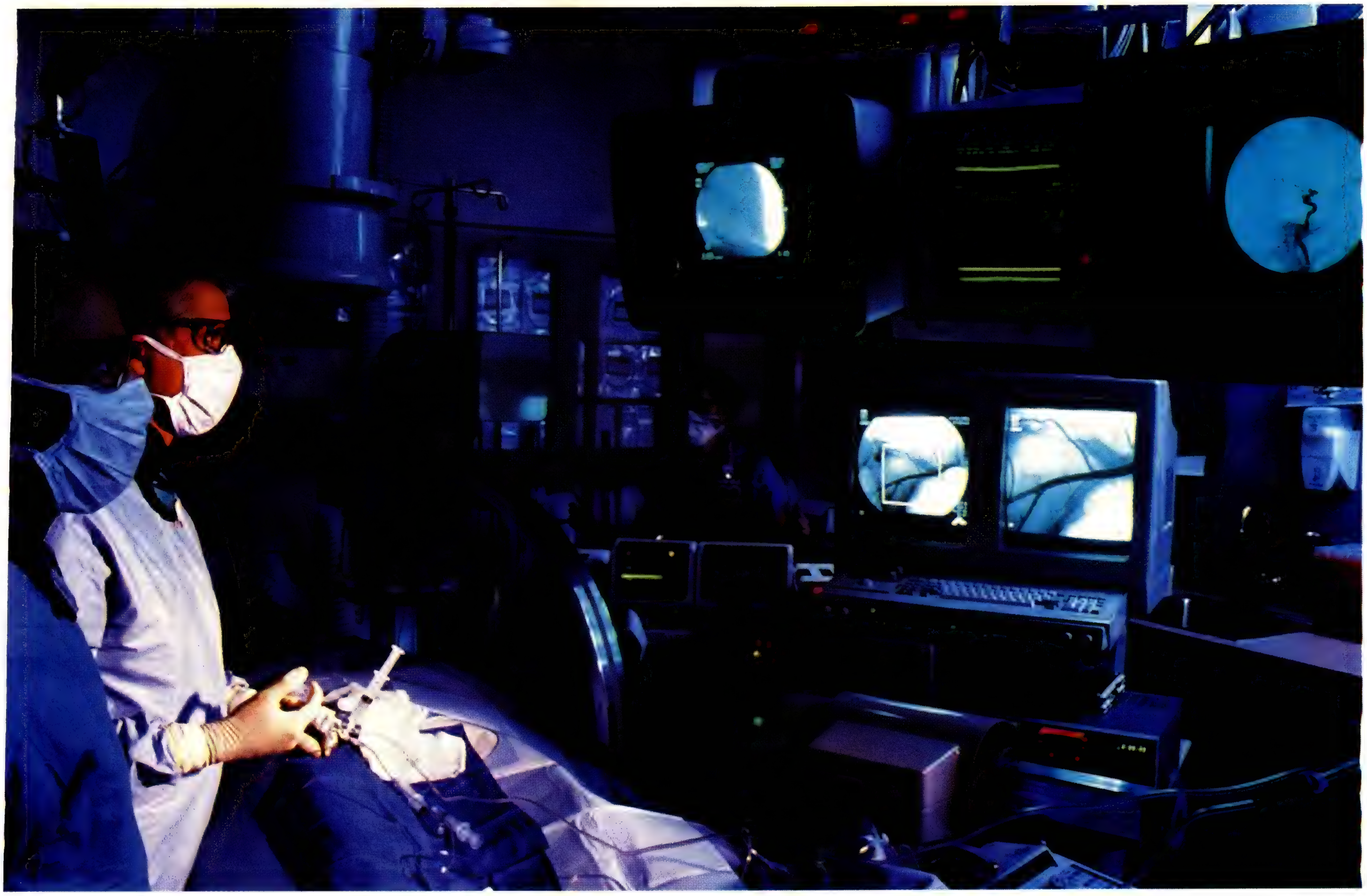

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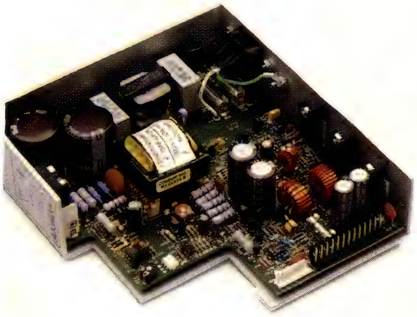

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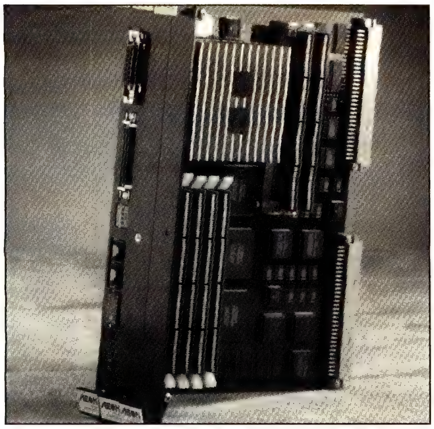
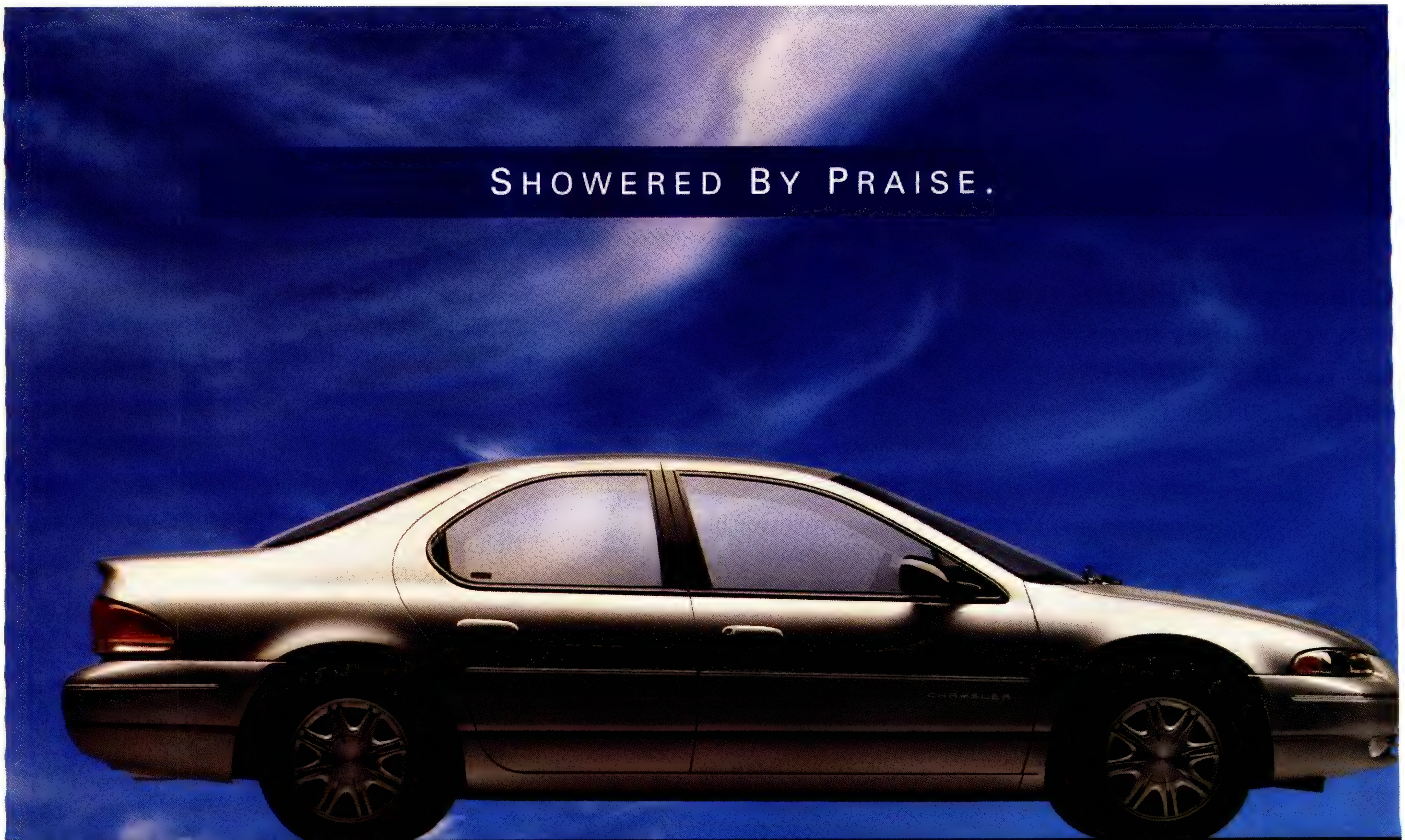


net, SCSI-2, and a 64-bit VMEbus interface. Other features include six independent 32-bit counter/timers, a 32-bit, 33-MHz local I/O bus, a 128-bit local bus with parity for processor-to-secondary cache and main-memory data exchange, and four RS-232C ports. From $11,995. **Aeon Systems Inc**, Albuquerque, NM. (505) 828-9120. **Circle No. 480**

Windows-based development tools and operating system for Intel and Motorola processors. The VRTXsa Developer's Kit for Windows is available for the Motorola 68000/68300 processor family or for protected-mode applications using the Intel 80386, 80486, or Pentium processors. The kit includes the company's C compiler; the Xray debugger for cross-development and debugging of VRTXsa applications; the VRTXsa real-time operating-system kernel for task scheduling, memory management, and communications; and a board-support package for a variety of single-board computers. The developer's kit for either Motorola and Intel processors costs $5800. **Microtec Research Inc**, Santa Clara, CA. (408) 980-1300. **Circle No. 481**

Device generates encrypted signals for remote, keyless entry applications. The HiSec Rolling Code Generator provides a different signal with each transmission, offering improved security over keyless encryption systems that send a fixed code. The device combines the contents of several dynamic data registers in a nonlinear manner that produces an encoded output. Data in the registers comprise a mixture of user- and factory-programmable and randomized data. The data are encrypted by clocking through a nonlinear logic block and feeding part of the output back to produce the final result. The device costs $1.50 (OEM) for a turnkey solution. **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959. **Circle No. 482**

Logic-test systems let you store or generate up to 1 million samples. The logic-analyzer version of the ET-1MEGplus provides 16 logic-analyzer channels operating at 25 MHz or eight channels at 50 MHz. The waveform-



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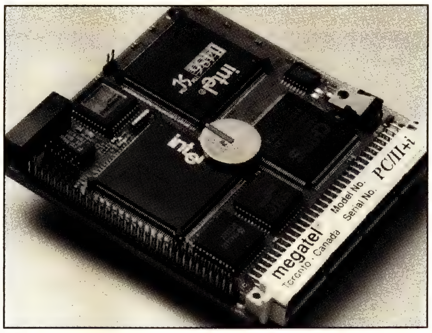
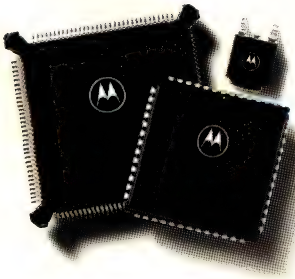
generator version provides 16 digital channels operating at 25 MHz or two analog channels. You can use other boards together for up to 64 digital channels of waveform generation or logic analysis. The logic analysis version also provides two clock qualifiers, a trigger qualifier, and multilevel triggering. The logic analyzer system costs $6295, and the waveform generator system costs $6595. **Emulation Technology Inc**, Santa Clara, CA. (408) 982-0660. **Circle No. 483**

AT-compatible SBC suits embedded-control applications. The AT-compatible PrimePlus single-board computer (SBC) comes in a 8×9-in. form factor. In addition to standard processor and I/O functions, the board has a ROM disk, SVGA graphics for driving CRTs and LCDs, key-switch scanning, a watch-dog timer, two RS-232C/422/485 ports, power management, and expansion capability for both standard ISA cards and the company's miniature expansion modules. The board costs $571 (100). **Dovatron International Inc**, Longmont, CO. (303) 772-5933. **Circle No. 484**



Single-board computer has 486DX in a PC/104-compatible module. The PC/II+i OEM2-4/104F module comes with either a header- or socket-style, 16-bit PC/104 interface. An ISA bus-compatible format is also available. The 4×4-in. board includes a CPU, a local-bus super-VGA video/LCD controller, an Ethernet interface, SCSI, floppy-disk and serial/parallel ports, 2 Mbytes of flash disk, a 32-bit DRAM data bus, an AT-compatible BIOS, and a built-in 8-kbyte cache with floating-point unit (FPU). The board operates from a single 5V power supply and requires 6W. It costs $1495. A 386SL version without an FPU and a cache starts at $995. **Megatel Computer Corp**, Weston, ON, Canada. (416) 245-2953. **Circle No. 485**

Graphical programming environment for developing signal- and image-processing applications. The ProtoPIPE graphical development environment includes a multiformat data viewer and a library of >200 signal- and image-processing algorithms and utilities. You create the application by graphically connecting the algorithms



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in an object-oriented design window. The software runs under SunOS 4.x and Solaris 2.x. A single-user floating license costs $10,000. The company also offers an Sbus card with a TMS 320C80 processor that provides 1 billion operations/sec. The S/IP80 card accelerates ProtoPIPE and includes a multistandard video digitizer and audio codec. The S/IP80, including the ProtoPIPE graphical programming environment, costs $27,000. **General Imaging Corp**, Billerica, MA. (508) 262-2262.

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ICE supports i960 Jx RISC processors. The TMax 5302 in-circuit emulator (ICE) accommodates the i960 JA's 3.3V operation and the JD's clock-doubled operation. Features include real-time processor emulation and tracing, complex-sequential-event/breakpoint capability, register and memory access, up to 8 Mbytes of emulation memory, source-level debugging, a high-speed parallel interface, and a bit-image display. The device lets you upgrade earlier versions of the modular TMax 5000 emulation systems. From $30,000. **Topmax Corp**, Mesa, AZ. (602) 730-2530.

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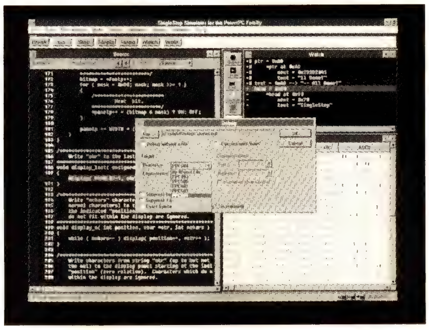

Software-development system simulates and debugs embedded-PowerPC applications. SingleStep for embedded PowerPC-applications has an instruction-set simulator that executes >7500 instructions/sec. The development system is compatible with the 600 series PowerPC devices developed by Apple Computer, IBM, and Motorola; the 500 series from Motorola; and the 400 series Embedded Controller from IBM Microelectronics. The tool supports the emerging EABI and ELF/DWARF object-file standards for embedded-PowerPC applications, allowing it to work with most embedded-PowerPC compilers. An instruction-trace buffer holds approximately 1 million instructions. Single-user licenses start at $1500. **Software Development Systems**, Oak Brook, IL. (708) 368-0400.

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Burst-mode EPROMs allow rapid data transfer for PowerPC and 68000 family processors. The NM27P6841 EPROM has a glueless burst data-transfer mode that executes four synchronous data transfers in a

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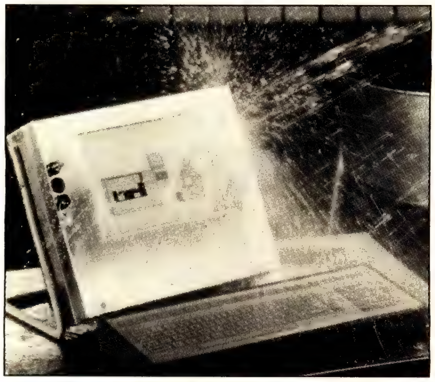
cycle. The device supports 4-1-1 burst data transfers at 25 and 33 MHz, avoiding the need to use shadow RAM. The system comes in a PLCC and costs $5.75 (10,000). **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959. **Circle No. 489**



Operator interface meets NEMA 4 standards. The Kontron Operator Interface comes in a stainless-steel case and is sealed against water and corrosive chemicals. Depending on the application, the operator interface can include simple, connector-protection, tight seals or a waterproof NEMA 4PG assembly. The unit is based on the 50-MHz 486DX2 processor and has an optional monochrome or color touch-screen. The standard version offers 4 Mbytes of DRAM expandable to 32 Mbytes, two half-length AT expansion slots, a Centronics port, two serial ports, and a PS/2 mouse interface. Mass-storage options include an internal 130- or 500-Mbyte hard-disk drive and a 2.5- or 10-Mbyte silicon disk. From $4965. **Kontron Electronic Corp**, Newport Beach, CA. (714) 851-1872. **Circle No. 490**

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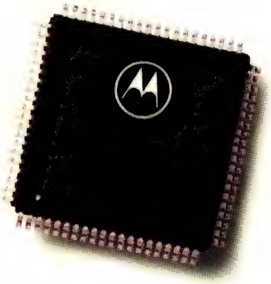

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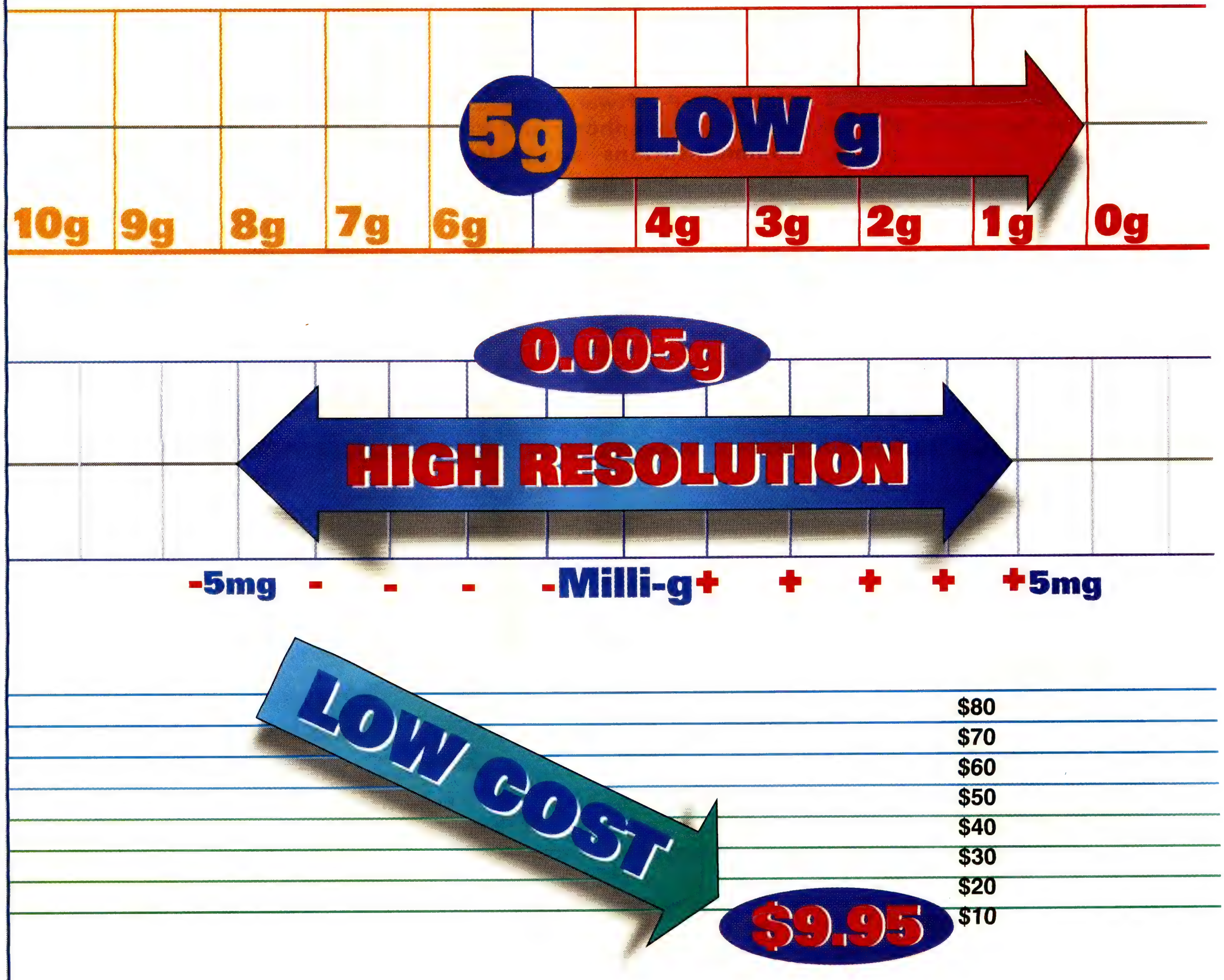

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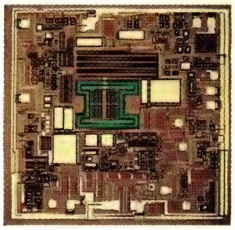

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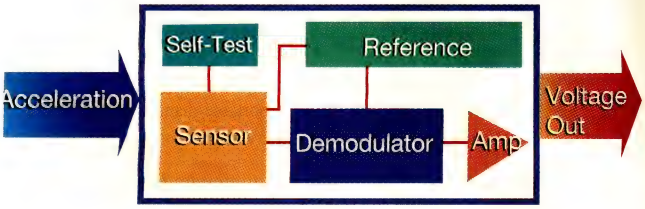

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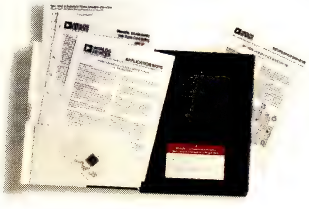

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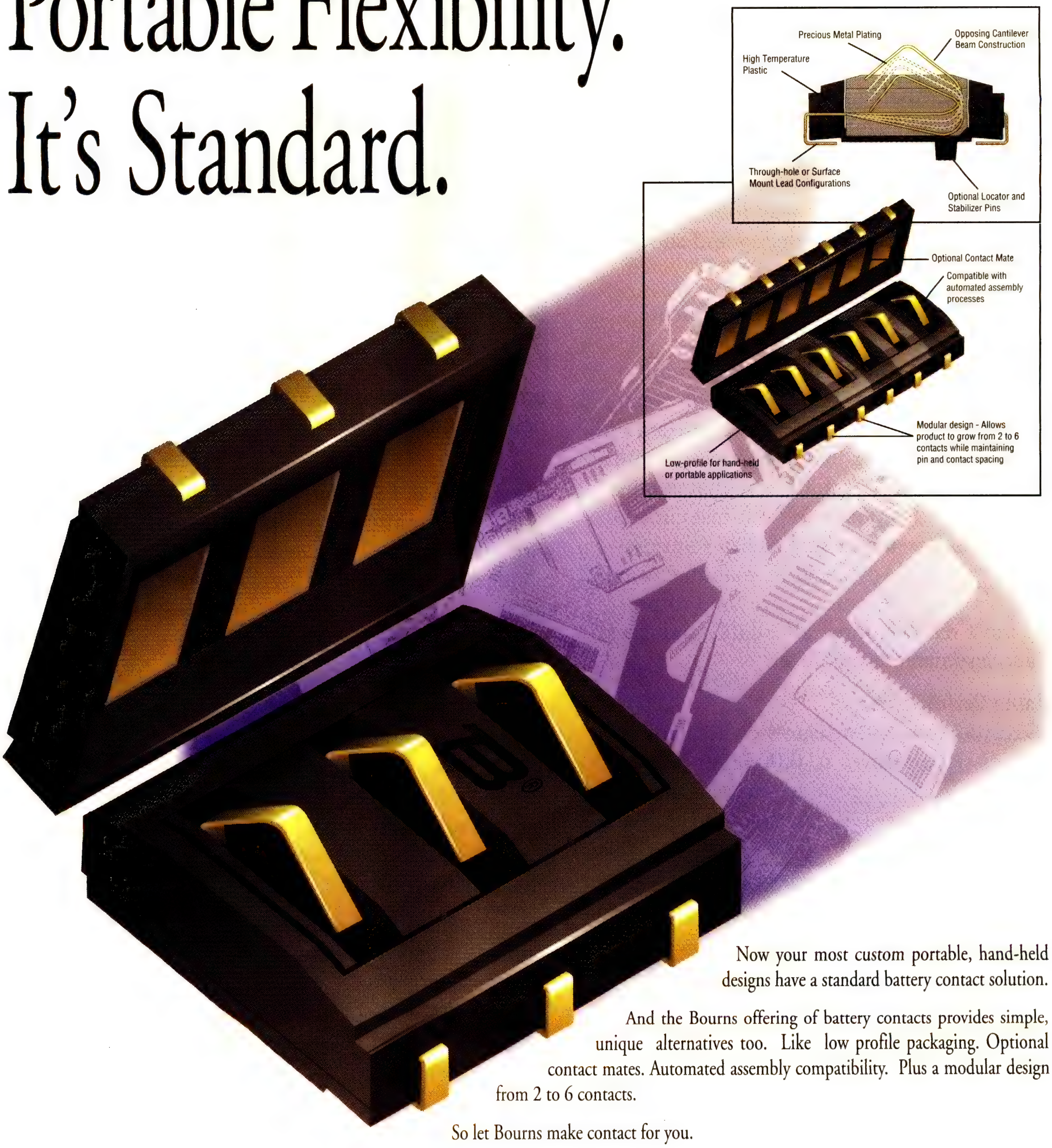
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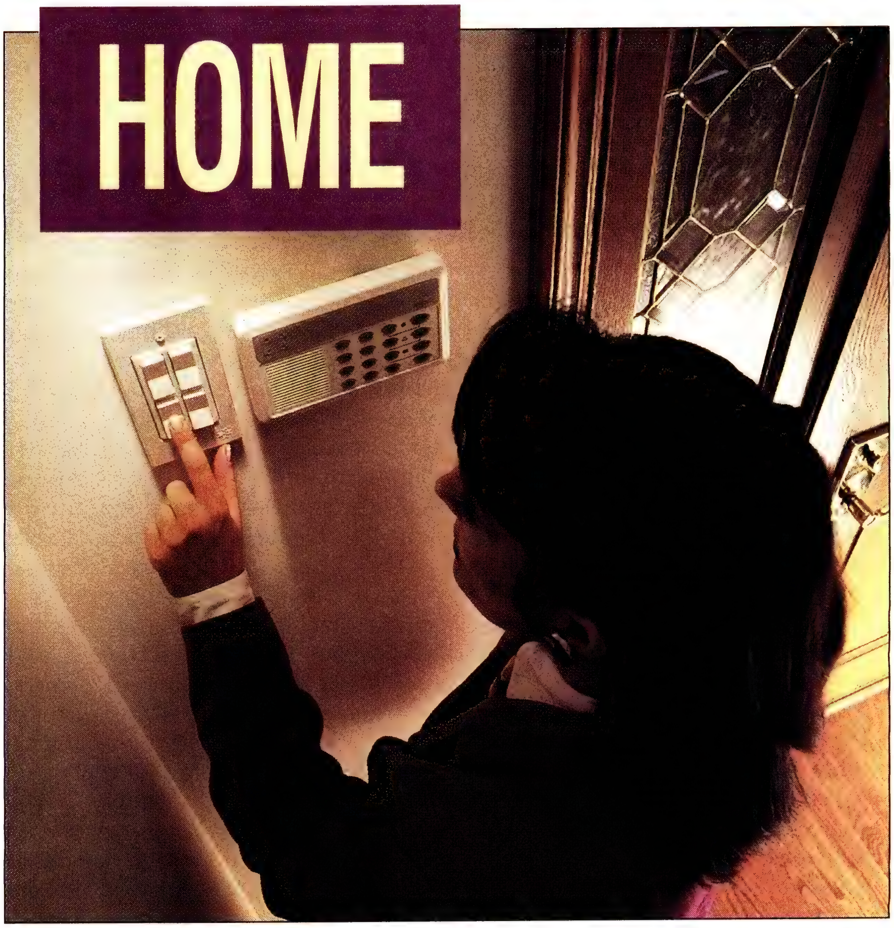
HOME-AUTOMATION BUSES: PROTOCOLS REALLY HIT HOME

Buses using wired and wireless technology—including IR, narrowband, and spread-spectrum communication—are bringing entertainment, security, and energy conservation to the home. But, even as several architectures vie for dominance, the industry keeps searching for that "killer application."

DAN STRASSBERG, SENIOR TECHNICAL EDITOR



In this Smart House system, entering a personal-identification code disables the security system, turns on selected lights, and changes the thermostat settings. (Photo courtesy of Molex)

Designers of buses and protocols to automate people's homes have taken on quite a challenge. Home-automation systems handle tasks as complex as those in industry but must cost much less. Some obstacles are unique: Few home owners want electricians to tear apart existing houses to install control wiring. Reliable implementation of power-line data communication, the "obvious" alternative to rewiring, has proven devilishly tricky. Meanwhile, wireless approaches present problems of their own. Today, three fairly new home-automation standards aim to capture a market still dominated by X-10, a protocol first deployed almost two decades ago.

Home-automation proponents predict that, from the widespread use of demand management—a scheme that employs technology to help utility companies and consumers reduce peak demand—will flow a torrent of ideas for convenient and lucrative new applications. (See **box**, "Demand management: home automation's 'killer app'?".) These applications would be impractical if the various elements of home-automation systems could not communicate freely. Open and reasonably priced communication among products from multiple vendors is what home-automation protocols are all about.

There are four major contenders among home-automation protocols:

- Echelon Corp's LONworks,
- The Electronic Industries Association's CEBus (EIA IS-60),
- Smart House, which Smart House LP (Limited Partnership) created for the National Association of Home Builders,
- X-10 (USA) Corp's X-10 protocol.

Table 1 summarizes key characteristics of the first three protocols.

HOME-AUTOMATION BUSES

Of the four protocols, X-10 is by far the simplest and oldest. It first appeared in 1978, and field experience with it far exceeds experience with the other three technologies combined.

LONworks is the only one of these protocols that has found wide use outside of the home. Echelon reports that over 500,000 LONworks nodes have been installed, mostly in factory-automation applications, and that at least 75,000 new nodes are being installed each month.

In larger buildings, especially commercial ones, several protocols compete, including a host of "fieldbus" standards (**Ref 8**). One standard specifically designed for automation of commercial buildings is the building automation and control network (BACnet) protocol (**Refs 1**, **2**, and **3**). The organization behind BACnet is the American Society of Heating, Refrigerating, and Air-Conditioning Engineers (ASHRAE).

In the United States, automating existing homes is—potentially, at least—a market about 100 times the size of the market for automating new homes. Because wiring installation is such a huge headache in existing homes, the industry has developed several communication techniques that don't require special wiring. Sending data over the ac power line is the oldest such approach. The earliest power-line communication systems (X-10, for example) used narrowband techniques. More recently, systems have used direct-sequence or chirp spread-spectrum modulation (**Ref 10**). Spread-spectrum technology is at the heart of CEBus' power-line communication capability and, along with a new, advanced narrowband design, is an option under LONworks.

Other approaches that avoid special wiring include RF and IR wireless communication. The developers of both the CEBus and LONworks standards envision RF and IR communications. X-10 Corp is active in both of these wireless

DEMAND MANAGEMENT: HOME AUTOMATION'S "KILLER APP?"

Suppliers of home-automation equipment look to energy conservation as a key factor in expanding the market. Utilities must size their generating capacity to handle peak loads and have a strong incentive to get customers to reduce their peak utility demand. If they can persuade customers to shift some of their power use to times when demand is lower, the utilities can avoid large capital outlays for added capacity. To achieve this objective, power companies are willing to share their savings with customers. In fact, some utilities even help customers pay for home-automation equipment that reduces peak demand.

Enter demand management: Under this concept, in return for a lower rate, customers agree, say, to run hot-water heaters only at times of off-peak demand. But what happens on the night when the boss comes over for dinner? On that night, a customer might be willing to pay extra to have abundant amounts of hot water for last-minute dishwashing and cleanup chores just when everyone else in town is using energy for cooking. An interactive system can solve the problem. With such a system, a power company might send signals to a water heater telling it when it can and should not run. For a price, a customer, perhaps with the aid of a remote control and special screens displayed on a TV, could override those signals.

You can conceive of relatively low-tech approaches that accomplish much the same thing. A 24-hour timer could shut down the water heater during peak-demand periods. A user could override such a shutdown by pushing a button on the water heater. The electric meter could separately track kilowatt-hours consumed during the parts of the day when different rates are in effect. A backup battery could keep the clocks in the water heater and the electric meter running during power outages. This low-tech approach does lack a few features, though. It can't easily adjust the peak-demand schedule, for example, when daylight-saving time begins and ends. It also cannot shut down whole-house air conditioners on hot days when demand threatens the power grid.

Although electric companies probably have the strongest incentive to institute demand management, they are not the only utilities interested in home automation. The Gas Research Institute, an organization created by the natural-gas industry, chartered a 1993 study by consulting company and system developer Diablo Research Corp. The study culminated in the publication of a detailed technical report on home-automation buses (**Ref 4**).

Utilities that supply natural gas and water are just as interested in reading utility meters from remote sites as electric companies are. Remote-meter-reading technology is closely related to home-automation protocols. Interesting battle lines are being drawn in this area of home automation. Telephone companies have much of the infrastructure utilities need to read meters remotely and to send and receive the control signals that demand management requires. However, utility companies appear more likely to hook up with cable-TV operators to meet their remote-control and communications requirements.

One of the reasons for the utilities' preference for cable-TV companies over phone companies relates to local telephone tariff structures. If utilities use the local telephone system for automatic meter reading, each reading requires a telephone call. Most tariffs require commercial users to pay for individual calls. Compared with the current system of sending people to homes to read meters, a scheme based on individual calls would not save utilities large amounts.

Another problem is technological. Telephone systems lack a mechanism for broadcasting messages to large groups of users. For demand management, utilities would like to be able to broadcast messages telling appliances when to shut down and when it's OK to power up again. This arrangement would allow simple, inexpensive appliances with little or no built-in intelligence. The telephone system's lack of a broadcast capability would force the appliances themselves or a controller in each house to keep track of the shutdown schedule. Of course, a low-tech demand-management approach could do much of the job.

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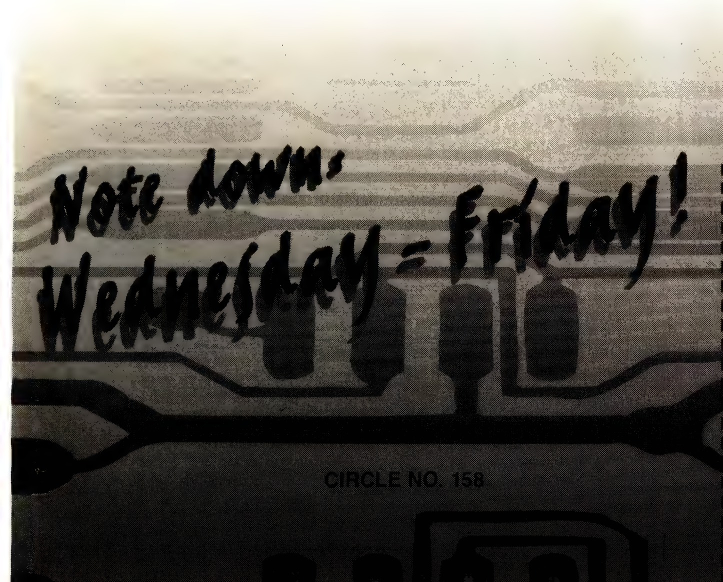

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technologies and has used them in some products that also incorporate the power-line-based X-10 protocol.

Many vendors and installers assemble systems using proprietary protocols. Such protocols abound in home-security applications, such as intrusion-, smoke-, and fire-detection systems. The proprietary schemes range from simple (a contact closure represents an alarm condition) to elaborate and from loosely defined to fully specified. In the installed base of home-automation systems, proprietary protocols are the norm; they've been around for decades, even if nobody dignified them with the name "protocol." Because multivendor protocols are newer, they are an exception to the norm. This article discusses only major multivendor protocols.

Authors who discuss home-automation protocols (**Refs 4, 6, 7, and 9**) almost always begin by declaring that comparisons are inappropriate—that comparing protocols is like comparing apples and oranges. That said, the authors proceed to compare the protocols.

X-10

X-10 owes its low cost at least partly to its simplicity. The abundant experience that users and installers have with X-10 is both a strength and a weakness; not everyone who has used X-10 likes it. In most X-10 installations, 120-kHz AM signals superimposed on the ac power line carry all messages. Whereas most other home-automation systems require professional installation, you often don't need to be a do-it-yourselfer to install a system based on power-line communication. Thus, consumers can set up X-10 systems themselves. Unfortunately, the reliability of X-10's simple protocol varies significantly among installations.

Today, designers understand much better than they did in 1978 just how terrible power lines are for transmitting signals. Indeed, power lines are probably a poorer transmission medium now than they were in the late '70s. Switching power supplies, which were recently introduced into homes, inject high-frequency noise onto ac lines, thus degrading the S/N ratio. To improve reliability, X-10 has made many refinements over the years but has retained its simple modulation scheme and generally has kept new units compatible with older products. Thus, you often can't tell which improvements a unit incorporates; if you have problems, you are likely—perhaps wrongly—to indict the whole X-10 line.

The most familiar embodiment of X-10 is the family of lamp- and appliance-control modules and control centers sold under the X-10 Powerhouse brand name. X-10 (USA) Inc's Asian affiliates manufacture these units as well as ones

TABLE 1—A COMPARISON OF CEBUS, LONWORKS, AND SMART HOUSE

	CEBus	LONworks	Smart House
Maximum number of nodes	61,000	Almost 10^{19}	900
Media supported	Power line, twisted pair, coaxial cable, RF, IR; fiber-optic cable (eventually)	Power line, twisted pair, RF; third-party transceivers support additional media	Custom-made wiring available from three sources
Data rate for control and communication	10 kbps	610 bps to 1.25Mbps	50 kbps
Support for high-speed data	Logical and electrical-channel allocations and media specifications for video, audio, and data distribution; standardized resource-allocation protocols	No specifications for video or audio channels	Coaxial distribution system
Ease of use: development	Big learning curve for network protocol; development tools reduce learning time	Development tools easy to use; no need to learn network-protocol details	Development tools are available
Ease of use: production	Maximum hardware flexibility; µP of 8 bits or more required	Two custom ICs from two manufacturers	Two custom ICs from Smart House
Ease of use: installation	Prewired connection or on-site association-algorithms	Varies: Equipment manufacturers can sometimes preinstall; users can install; professional installation can be required	Addressing tool required to initialize some components; Databases can be established on site or remotely
Target applications	Existing and new homes	Existing and new homes,commercial and industrial buildings, industrial automation	Residential (new homes, primarily), some light commercial buildings
Relative cost	Low to moderate	Low to moderate	Moderate to high

*Adapted from "Home-automation systems in North America: an analysis of the three main contenders," by Diablo Research Corp, distributed by the Gas Research Institute.

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sold under other names, including Decora Home Control from Leviton Manufacturing Co. Because X-10 is available from many companies with broad distribution, we include it with the major multivendor protocols.

Although data transmission under the X-10 protocol is not fast, it is usually fast enough for the target application. Except for the message preamble, which packs 4 bits into two ac-line cycles, transmission proceeds at 1 bit per line cycle. A message comprises 13 bits—the 4-bit preamble, a 4-bit house code (which the user sets to avoid interfering with systems in nearby houses), a 4-bit unit/function code, and 1 bit that indicates whether the unit/function code represents a unit number or a function. Examples of functions are on, off, brighter, and dimmer. This arrangement allows up to 16 modules, each of which can respond to up to 16 commands. By using multiple house codes, systems can include more than 16 modules.

To improve reliability, a packet contains two identical messages, which are concatenated without a gap. A command consists of two packets transmitted with a gap of at least three line cycles. In the first packet, the unit/function code indicates which unit is being addressed; in the second packet, the unit/function code represents the function. A command requires at least 47 cycles and takes nearly 0.8 sec at 60 Hz.

AM 120 kHz

Each bit is transmitted as an ~2-msec burst of an amplitude-keyed, 120-kHz carrier whose amplitude in the on state is 6V p-p in the United States and 2.8V in Europe, where electromagnetic-compatibility regulations are tougher. The actual amplitude depends strongly on the line impedance at 120 kHz, although some modules use feedback to stabilize the amplitude. The start of each 120-kHz carrier burst coincides with a line-voltage zero crossing, so the burst repeats twice per cycle in single-phase systems and up to six times per cycle in three-phase systems. To distinguish the preamble from normal data, the bits transmitted during the two halves of preamble line cycles need not be the same.

Most US houses use split-phase ac (120V from each side to neutral). When wiring houses, electricians try to balance the loads. Some 120V outlets connect from one phase to neutral; others connect between the opposite phase and neutral. High-power loads, such as electric ranges and clothes dryers, connect from phase to phase, across 240V. When the 240V loads are off, the impedance from phase to phase is quite high. Thus, if you plug an X-10 controller into a 120V outlet, the chance is only about 50% that the controller's signal can reach a control module plugged into another 120V outlet elsewhere in the house. To solve this problem, X-10 sells units that electricians can connect from phase to phase to provide a low impedance at 120 kHz.

Over the years, X-10 has made many product improvements, including adding metal-oxide varistors to prevent damage from transient spikes, changing to triacs that withstand the momentary short circuits that can occur when incandescent lamps burn out, and adding automatic gain control to some modules. X-10 has also devel-

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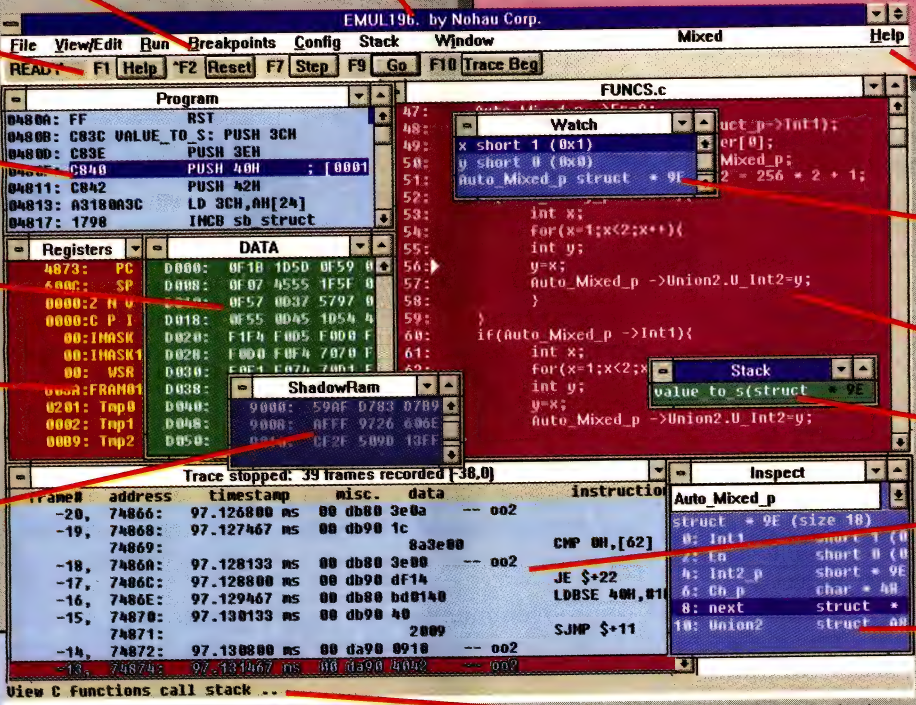

```
0480A: FF              RST
0480B: C83C VALUE_TO_S: PUSH 3CH
0480D: C83E            PUSH 3EH
       C840            PUSH 40H      ; [0001
04811: C842            PUSH 42H
04813: A3180A3C        LD 3CH,AH[24]
04817: 1798            INCB sb_struct
```

```
4873:   PC
        SP
0000:Z N V
0000:C P I
  00:IMASK
  00:IMASK1
  00:  WSR
     :FRAM01
0201: Tmp0
0002: Tmp1
00B9: Tmp2
```

```
D000:  0F18 1D5D 0F59
D008:  0F07 4555 1F5F
       0F57 0037 5797
D018:  0F55 0D45 1D54
D020:  F1F4 F0D5 F0D0
D028:  F0D0 F0F4 7070
D030:
D038:
D040:
D048:
D050:
```

```
9000:  59AF D783 D7B9
9008:  AFFF 9726 606E
       CF2F 509D 13FF
```

```
47:
48:                                   uct_p->Int1);
49:                                   er[0];
50:                                   Mixed_p;
51:                                   2 = 256 * 2 + 1;
52:
53:         int x;
54:         for(x=1;x<2;x++){
55:         int y;
56:         y=x;
57:         Auto_Mixed_p ->Union2.U_Int2=y;
58:         }
59:     }
60:     if(Auto_Mixed_p ->Int1){
61:         int x;
62:         for(x=1;x<2;x
            int y;
            y=x;
            Auto_Mixed_p ->Union2.U_Int2=y;
```

```
x short 1 (0x1)
y short 0 (0x0)
Auto_Mixed_p struct  * 9E
```

```
value to_s(struct  * 9E
```

```
Trace stopped:  39 frames recorded [-38,0]
frame#  address   timestamp       misc.  data              instruction
 -20,   74866:    97.126800 ms    00 db80 3e0a    -- oo2
 -19,   74868:    97.127467 ms    00 db90 1c
        74869:                            8a3e00           CMP 0H,[62]
 -18,   7486A:    97.128133 ms    00 db80 3e00    -- oo2
 -17,   7486C:    97.128800 ms    00 db90 dF14             JE $+22
 -16,   7486E:    97.129467 ms    00 db80 bd0140           LDBSE 40H,#1
 -15,   74870:    97.130133 ms    00 db90 40
        74871:                            2009             SJMP $+11
 -14,   74872:    97.130800 ms    00 da90 0910    -- oo2
 -13,   74874:    97.131467 ms    00 da90 4042    -- oo2
```

```
Auto_Mixed_p
struct  * 9E (size 18)
 0: Int1
 2: Ln                short 0 (0
 4: Int2_p            short * 9E
 6: Ch_p              char * 48
 8: next              struct  *
10: Union2            struct  A8
```

```
View C functions call stack ..
```

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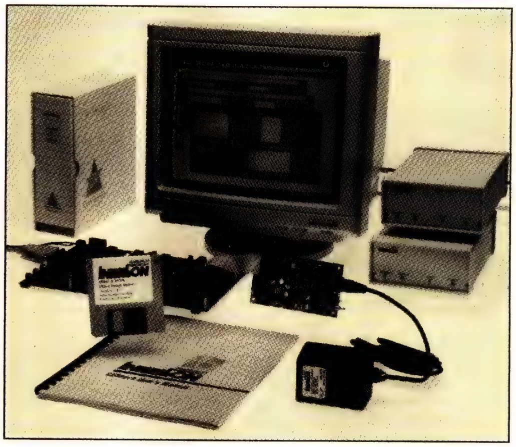
oped an extended protocol that allows for larger systems with more functions. Moreover, certain X-10 units can now acknowledge the receipt of commands. Controllers designed to work with these modules can retransmit a command until they receive acknowledgment. This feature addresses an often-heard complaint about X-10—that modules fail to turn on and off.

Nevertheless, X-10 faces several problems in expanding its user base. The company must convince potential users that it has overcome the reliability problems that have plagued its technology. Moreover, the X-10 protocol is proprietary, and the company does not currently license others to use it. As noted, though, X-10 (USA) incorporates its technology in products it builds for other companies. It also designs custom products to its partners' specifications. However, unless their applications appear able to generate enough volume to interest X-10 in custom designs, potential users for whom existing X-10 products don't work must look to other—often more expensive—technologies.

X-10's policy of not licensing its technology contrasts sharply with the approaches used by backers of other home-automation protocols. Although only CEBus is in the public domain, manufacturers can license LONworks and Smart House. In most cases, license fees are built into the price of components used in products that support the standards. Moreover, even CEBus has some proprietary aspects. For example, it uses a patented chirp spread-spectrum power-line and RF-wireless communication scheme developed by Intellon. Like Echelon and Smart House LP, Intellon encourages others to use its technology in their products; the company receives royalties from the sale of ICs that implement its protocol.

SMART HOUSE

If X-10 is the Volkswagen Beetle of home-automation protocols, Smart House is the Mercedes Benz SL600. A Smart House system comprises five subsystems: control/communications, telecommunications, electrical energy, coaxial network, and gas energy. The gas-energy subsystem is optional. To a much smaller extent, so is the coaxial network, which distributes video, audio, and high-speed data. The coaxial network is a broadband RF distribution system, which interfaces with cable and broadcast TV.



These CEBus tools come from Intellon, the company that originated the bus' spread-spectrum power-line and wireless-RF communications technology.

The heart of a Smart House system is the control/communications subsystem, which transmits signals at speeds to 50 kbps. This subsystem includes the system controller, a 12V-dc power supply, cabling that distributes signals throughout the house, sensor outlets, and switches. Within the control/communications subsystem (from a logical standpoint) are branch/slave ICs that format messages, convert between serial protocols, implement node addressing, and provide a power-control interface. Physically, the ICs reside in the devices to which they interface—120V-ac convenience outlets, lamp dimmers, lighting fixtures, and points of connection to permanently wired appliances.

Although you can use conventional appliances in a Smart House system, the Smart House standard defines three other appliance classes: simple, normal, and complex. Appliances in all three of these classes interface with the three status lines and one control line of the Smart House appliance-channel connector. The last two classes require a Smart House appliance chip, which implements the physical and data-link layers of the Smart House appliance protocol. Complex appliances also require a μP.

The system controller is an electronics module and enclosure. It can manage communication and control power on up to 30 branch networks, each of which can have up to 30 nodes or attachment points. In addition, the system controller implements all protocols, executes programmed event/action sequences, manages system databases, and coordinates other functions.

Even the ac outlets are smart

The electrical-energy subsystem, which distributes 120 and 240V ac throughout the house, incorporates surge protectors and ground-fault interrupters on each branch. In a Smart House, wall switches do not switch ac power; they switch 12V dc. The system controller senses this dc and directs ac to the appropriate wall outlets, lighting fixtures, and permanent appliances. Outlets can sense whether a load is connected and can wait until a load is connected before applying power.

The control/communications subsystem implements a pair of 9600-bps RS-232D asynchronous serial channels. One of these channels is the sole interface between the control/communications and telecommunications subsystems. The second serial port lets service technicians access the system.

Smart House defines several cable types. Most messages travel among sensors, appliances, outlets, and the system controller on six-conductor cable. The telecommunications subsystem uses four twisted pairs. This subsystem can accommodate both analog and digital telephone devices, modems, dual-tone multifrequency decoders, and voice-response devices. In conjunction with the control/communications subsystem, the telecommunications subsystem permits telephone access to home-security functions and allows using the telephone for remote control of devices throughout the house.

One of the drawbacks of Smart House has been its cost. Installing Smart House during construction can add $20,000 to the cost of a home. To mitigate this problem, companies that supply Smart House products have

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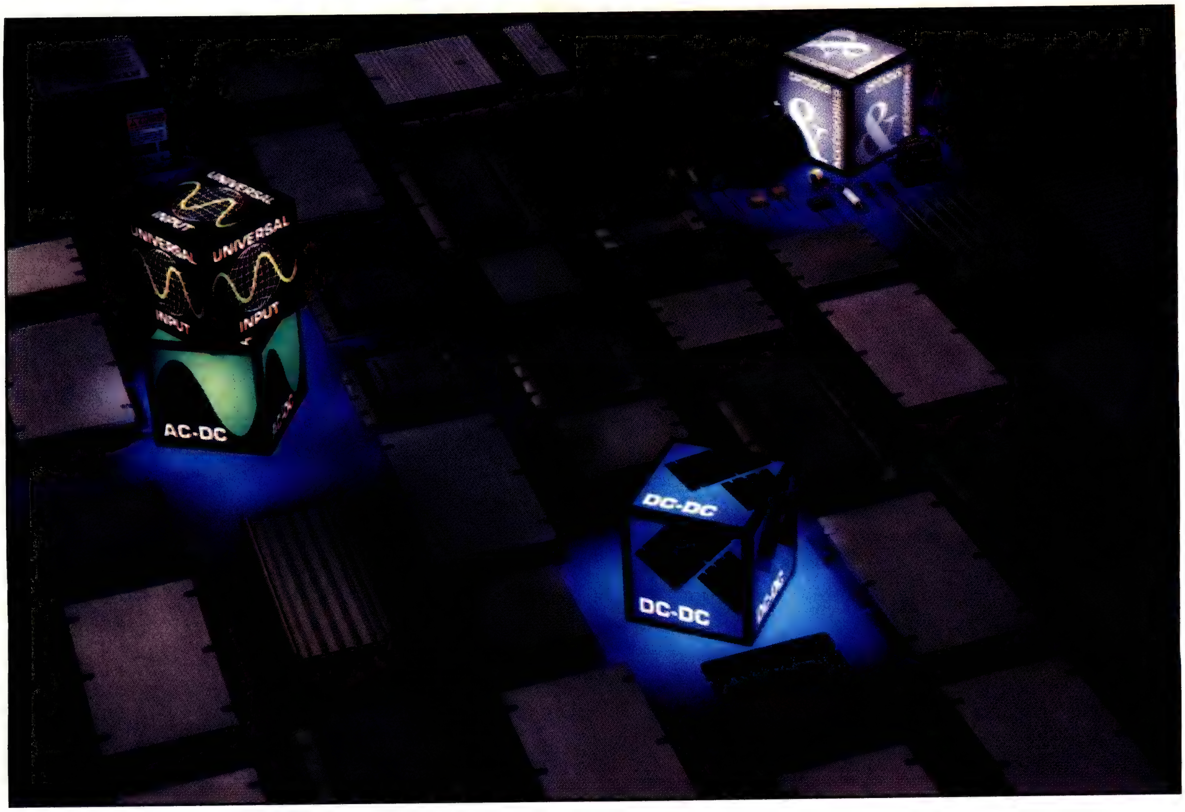

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developed the Smart-Redi program. Under Smart-Redi, a builder installs only certain portions of a Smart House system. Later, though, the purchaser can easily replace or modify items that do not fully implement Smart House. Smart-Redi requires buyers of new homes to pay only for those Smart House features they plan to use immediately plus a modest premium for products that allow upgrading without reconstruction or rewiring.

CEBus

CEBus, or EIA IS-60, encompasses two standards: one for low-speed (less-than-10-kbps) control, the other for high-data-rate signals—digital video, for example. The standard is comprehensive; the specification document is over 1000 pages long. CEBus products can implement only the low-speed portion of the standard or both the low- and high-speed portions.

Because CEBus is a peer-to-peer network, it does not require a system controller of the type that is at the heart of Smart House systems. CEBus offers a wide choice of low-speed signal-transmission media: power-line carrier (PLC), twisted pair, wireless RF, and IR. Higher speed data can travel on twisted-pair, coax, or fiber-optic cable, although the fiber-optic portion of the standard is not yet complete. Telephone service can share cables that contain four twisted pairs. Bridges or routers link the various media in a network.

The PLC technology uses a chirp spread-spectrum signaling technique, which Intellon patented. The chirps cover 100 to 450 kHz. Whereas some spread-spectrum systems make it virtually impossible for outsiders to intercept messages, the receivers in such systems take many milliseconds to lock onto signals. Intellon's priority wasn't a system that could provide high security, but one that could quickly transmit many messages. So, the CEBus PLC system uses carrier-sense multiple access with collision detection to control its nodes' access to the power-line medium.

Competitor Echelon has questioned the reliability of Intellon's first-generation chirp spread-spectrum hardware and has developed a narrowband power-line modem for LONworks. Echelon claims that its new modem is more reliable than either its own spread-spectrum power-line modems or Intellon's CEBus devices. Echelon now lets LONworks users choose either narrowband or spread-spectrum power-line modems.

Spread spectrum fights back

Intellon has not been napping, however. The company says it has found and fixed its technology's Achilles' heel: saturation of receiver front ends by high-amplitude narrowband noise sources. Intellon will soon announce second-generation chirp spread-spectrum CEBus modems that are backward-compatible with the company's earlier units. Intellon believes these modems are even more reliable than Echelon's new narrowband units.

CEBus is more than a power-line-communications technology. ISO's seven-layer reference model fully defines the protocol. A description of a CEBus "frame," or packet, gives an idea of the thoroughness and flexibility of the standard. A normal frame comprises eight sections: a preamble (PRE), a control byte, a destination address, a destination house code, a source address, a source house code, up to 32 bytes of information, and a frame-check sequence (FCS). Addresses and house codes can contain up to 16 bits.

Acknowledgment frames include the PRE, control, information, and FCS sec-

LOOKING AHEAD

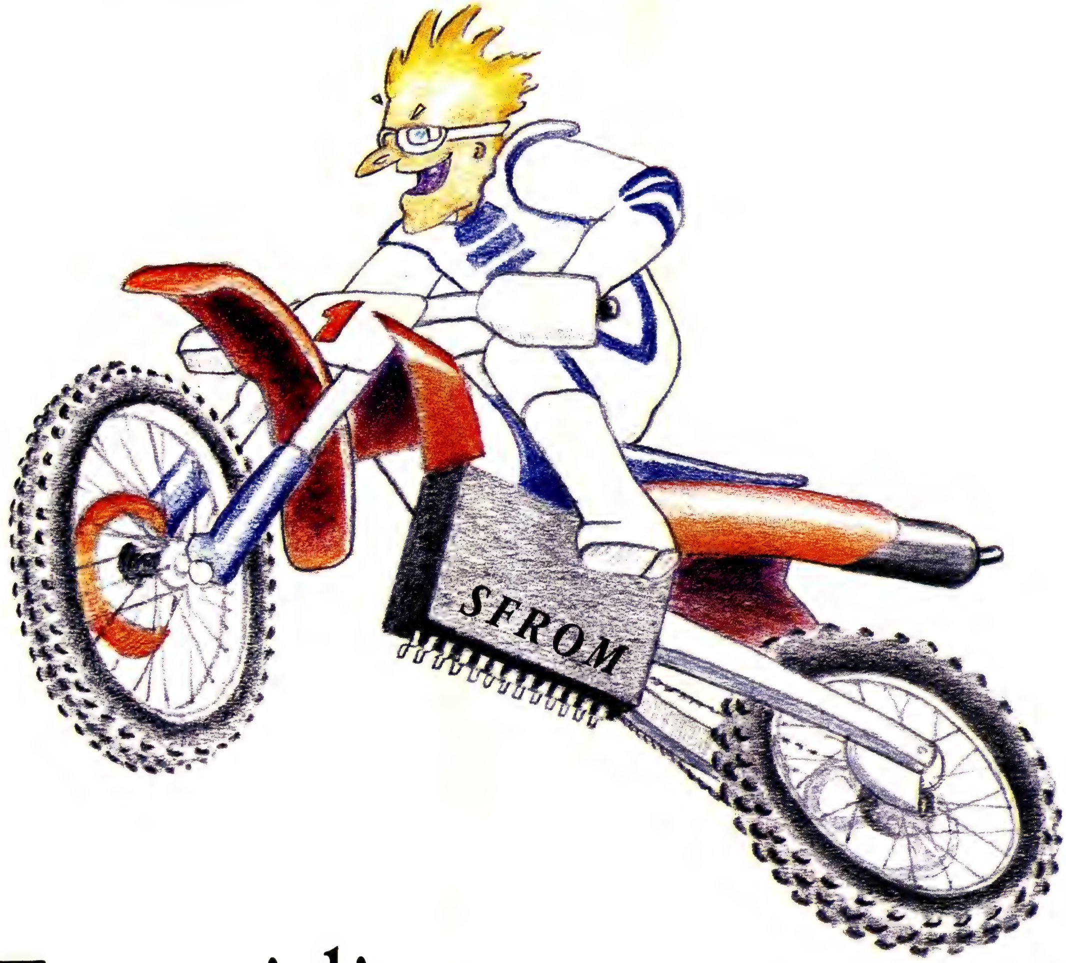
Industry observers are reluctant to pick a winner among CEBus, LONworks, and Smart House. Yet, when pressed, they give CEBus a slight edge, citing its open architecture and broad support. (See **Refs 4**, **6**, and **7**.) So far, though, CEBus is too new to lead in the number of installations. In fact, because CEBus products are only now beginning to appear, CEBus is currently in last place.

The same industry observers make a good case that the three protocols, along with X-10, will coexist. Technically, they can do so. Within a single house, you can install multiple systems, each using a different protocol and have all of the equipment work without interference. This does not imply interoperability among the protocols, however. Achieving interoperability would be desirable but requires further effort. Proponents of the several protocols are now beginning to focus on such efforts. Ultimately, one or more of the protocols might disappear as a separate entity but could live on as part of a broader standard.

Thanks to Echelon's aggressive promotion and its substantial and growing installed base in industrial applications, LONworks' longevity seems assured. Although LONworks would benefit from playing a major role in home automation, it can do just fine without the home market. Strangely enough, because LONworks doesn't need the home market, it just might be especially well-positioned to penetrate that market.

In picking a winner between CEBus and Smart House, a slight edge goes to CEBus. Smart House, despite a current lead in available products, is not as broad a standard as CEBus. Smart House doesn't include power-line, wireless-RF, or IR communications. Thus, in existing houses, installing Smart House requires major dislocations that, at least some of the time, CEBus can avoid. Smart House's requirement for a relatively expensive central system controller also biases the protocol toward the high end of the market.

Amp Inc, a provider of part of Smart House LP's funding and a large company with a broad line of Smart House products, says that it will offer products for any home-automation technology to which the company can justify committing. That means that, in addition to Smart House, Amp could commit to CEBus, LONworks, both of them, or something else—perhaps a standard embodying several of the protocols—that hasn't been formally proposed yet.



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tions. An acknowledgment frame usually contains no information and, at most, contains only 2 bytes.

CEBus is starting to gather momentum. The quarterly catalogs from Home Automation Laboratories (see **box**, "For free information…"), which heretofore have focused on products that support the X-10 standard, have recently started to include a few CEBus products as well. Moreover, each successive issue of the catalog includes a few more CEBus items.

LONWORKS

Echelon Corp's LONworks is the newest home-automation bus. Despite its relative newness, the system is complete. Echelon has done a thorough job of defining and documenting LONworks in terms that developers—both of applications and of compatible products—can easily grasp.

Moreover, Echelon has enrolled hundreds of partner companies (at last count, about 700) to offer LONworks hardware, development tools, and support. Part of the reason for Echelon's success in developing partnerships stems from the company's broad focus. LONworks is the only one of the multivendor home-automation protocols that aims at applications outside the home. LONworks has already achieved considerable success in industrial automation.

Like CEBus, LONworks is a peer-to-peer system and so requires no system controller. LONworks offers a wide variety of data rates and transmission media. Data rates range from hundreds of bits per second to 1.25 Mbps. Media include twisted pair, 49- and 450-MHz wireless RF, IR links, and the ac power line. One option is an RS-485 transceiver. Microsym offers a 1.25-Mbps fiber-optic transceiver.

At the heart of virtually every LONworks-compatible hardware unit is an Echelon Neuron IC. These chips, the 3120 and 3150, implement much of the LONworks protocol's lowest layers. In so doing, they greatly simplify the jobs of application developers, who need not worry about the minutiae of network interfacing.

Even though they share a peer-to-peer organization, CEBus and LONworks represent different philosophies of protocol design. CEBus appears to place high value on generality—on not establishing rules so specific to particular hardware or applications that they would limit opportunities for future growth. LONworks' developers, however, were more pragmatic. Although they did not turn their back on flexibility, they sacrificed some flexibility to achieve simplicity and ease of implementation.

These interconnection products from Molex are just a few of hundreds available from several sources for Smart House's four electrical and electronic subsystems.

Examples of LONworks application-focused approach include comprehensive sets of standard network-management and diagnostic messages and a set of standard network-variable types. These sets are extensible using a process that Echelon controls. **Ref 4** notes a possible shortcoming of Echelon's focused approach—LONworks' speed of response. According to the reference, an attempt to phase-control a triac via a LONworks network provided only about 1-msec resolution—not fine enough for the application.

The **references** and the **box**, "For free information…" are good places to begin searching for more detailed information on home automation. Companies that want to educate groups of employees on the technology can arrange for in-plant seminars. The Training Department, a consulting company, conducts such tutorials. Company President Grayson Evans says that his company has conducted more than 100 seminars on CEBus alone. EDN

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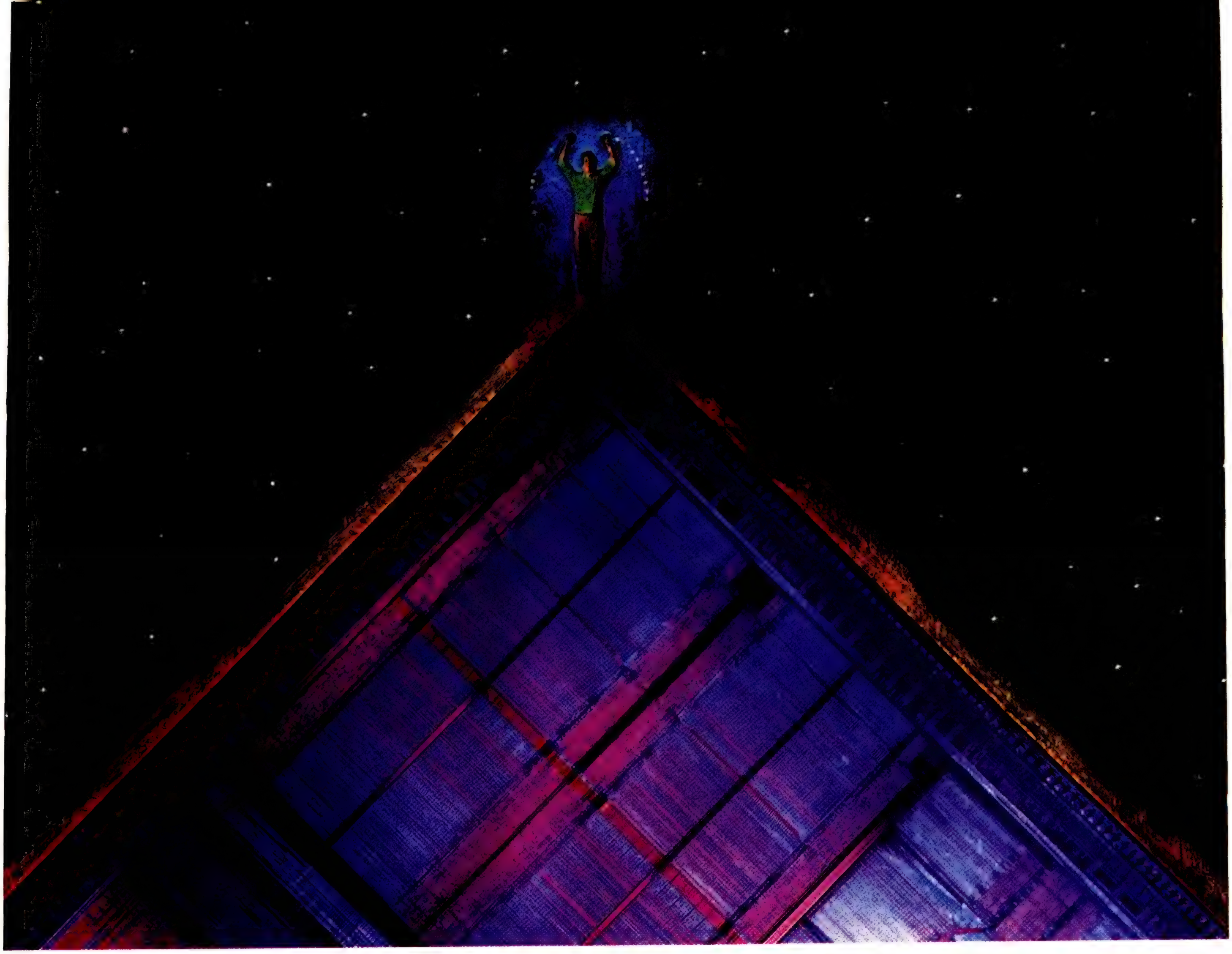

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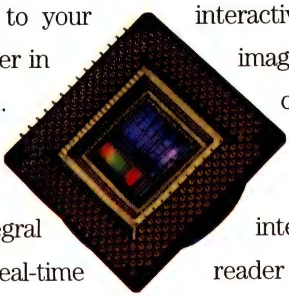

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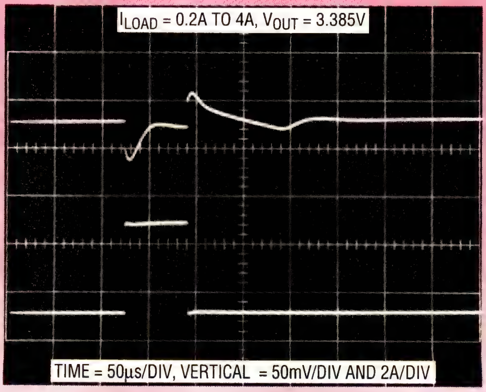

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Three-input supply powers 3.3V portables

LEN SHERMAN, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

The single-ended primary-inductance converter in **Fig 1** accepts input voltages ranging from 3 to more than 6V and produces a regulated 3.3V, 200-mA output. The converter accepts an input voltage from three sources: a 5V dc wall cube, a three-cell AA battery, and a lithium backup battery.

Unlike conventional boost regulators whose battery current continues to flow during shutdown (unless you add a cutoff switch), this circuit's output turns off fully in response to a shutdown command. And, unlike flyback-transformer regulators and combination step-up/linear regulators, **Fig 1** requires no transformers. Coils L_1 and L_2 should be the same type and have the same value, but coupling between them isn't required. You can wind the inductors on the same core for convenience, but the circuit works equally well if they are completely separate.

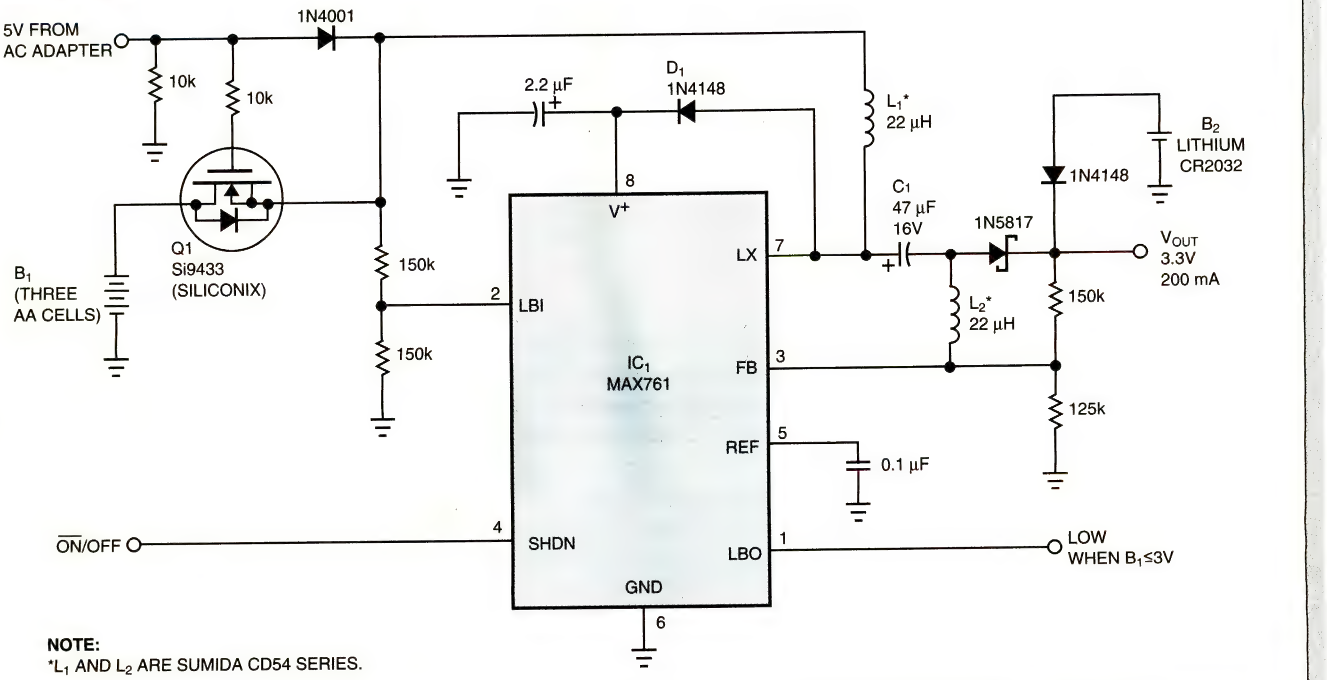
C_1 couples energy to the output and must have low equivalent series resistance (ESR) to handle the high ripple currents. Conversion efficiency with a low-ESR Sanyo OS-CON capacitor is 85%, which is 3% higher than with a less-expensive 1-µF ceramic capacitor. Tantalum capacitors are not recommended because they self-heat at high ripple currents.

During normal operation, the ac adapter's 5V output powers the circuit and turns off Q_1. Disconnecting the adapter removes 5V, turns on Q_1, and allows the three AA cells, B_1, to provide power. If the 3.3V output drops below 3V, a low-battery comparator in IC_1's step-up dc-dc converter alerts the system by driving LBO low. And for backup, a diode-OR connection allows an optional lithium battery (coin cell B_2) to provide load current at the 3.3V output.

As an added twist, D_1 provides a supply voltage for IC_1 (pin 8) by capturing the switching pulses at LX (pin 7). This voltage, which approximately equals the sum of V_{IN} and V_{OUT}, improves start-up capability under full load and improves low V_{IN} efficiency by boosting gate drive to the internal switching MOSFET. Maximum V_{IN} is limited to about 12V, which easily accommodates the three-cell battery. (DI #1686) EDN

To Vote For This Design, Circle No. 318

FIGURE 1



NOTE:
*L_1 AND L_2 ARE SUMIDA CD54 SERIES.

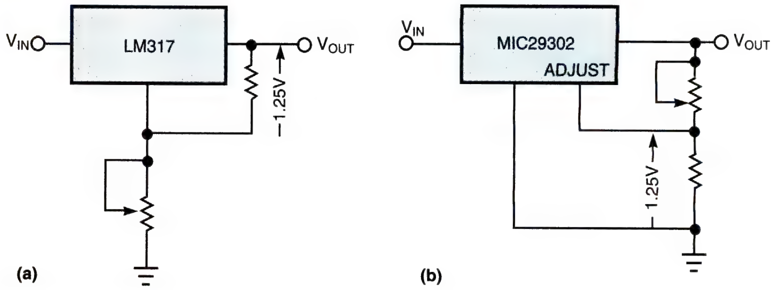
When the wall cube is disconnected, this single-ended primary-inductance converter draws power from a three-cell battery. An optional lithium battery backs up the 3.3V output.

Pass regulator's output ranges from 0 to 20V

MARVIN VANDER KOOI, MICREL SEMICONDUCTOR, SAN JOSE, CA

Adjustable-voltage pass regulators normally allow the output infinite adjustment between some maximum V_{OUT} and one bandgap voltage away from ground. The internal bandgap reference for the error amplifier limits the minimum output voltage. Some regulators have well-behaved, constant ground currents so that you can "float" the pass regulator on top of an adjustable resistor. This scheme requires a relatively high quiescent current to swamp out the pass regulator's ground current. Other regulators have a dedicated high-input-impedance adjust input and, therefore, a lower quiescent current. **Fig 1** shows both of these standard options. These designs produce quick and easily adjustable regulators, but their outputs can never be less than 1.25V, which is the zero-temperature-coefficient point of most semiconductor bandgap references found inside ICs.

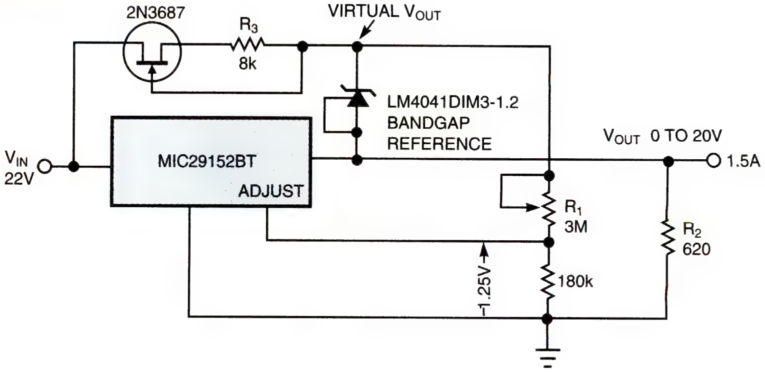
FIGURE 1



These designs provide quick and easily adjustable regulators, but their outputs can never be less than 1.25V.

Fig 2's alternative scheme shows a simple and practical single-supply pass regulator for variable output laboratory supplies and for fixed-output regulator applications requiring an output of less than 1V. The circuit uses a second bandgap reference (available in separate components in very small packages) to fool a regulator, and a feedback divider to make an adjustable supply that can supply a V_{OUT} of 0 to 20V. The circuit uses the second bandgap reference to translate the output of an adjustable regulator up to a "virtual V_{OUT}" and then uses that virtual V_{OUT} as the top of the feedback divider.

FIGURE 2



To make a pass regulator that's adjustable down to 0V, this circuit uses a stand-alone bandgap reference to translate the output of an *adjustable* regulator up to a "virtual V_{OUT}" and then uses this virtual V_{OUT} as the top of the feedback divider.

When R_1 goes to 0Ω, the output is 0V; the virtual V_{OUT} is one bandgap voltage above ground; and, therefore, the adjust input is also one bandgap voltage above ground. The regulator's error-amplifier circuitry is satisfied that both of its inputs are at one bandgap voltage and, therefore, it keeps the output voltage constant at 0V. The circuit fools the regulator into providing a lower than one bandgap output. The virtual V_{OUT} tracks any increases in R_1, albeit at a fixed one bandgap voltage above the actual V_{OUT}, and the pass regulator's output rises from ground. The maximum possible V_{OUT} equals the regulator's maximum input voltage minus the approximately 2V housekeeping voltage required by the current-source FET and the external bandgap reference.

The current source, composed of the 2N3687 JFET and R_3, provides approximately 77 μA—70 μA for the bandgap and 7 μA for the resistor string (approximately 100 times the nominal 60-nA input current of the pass regulator's adjust input). The optional R_2 bleeds off the 70 μA from the external bandgap reference if no load is present and the circuit is set for 0V out. (DI #1687) EDN

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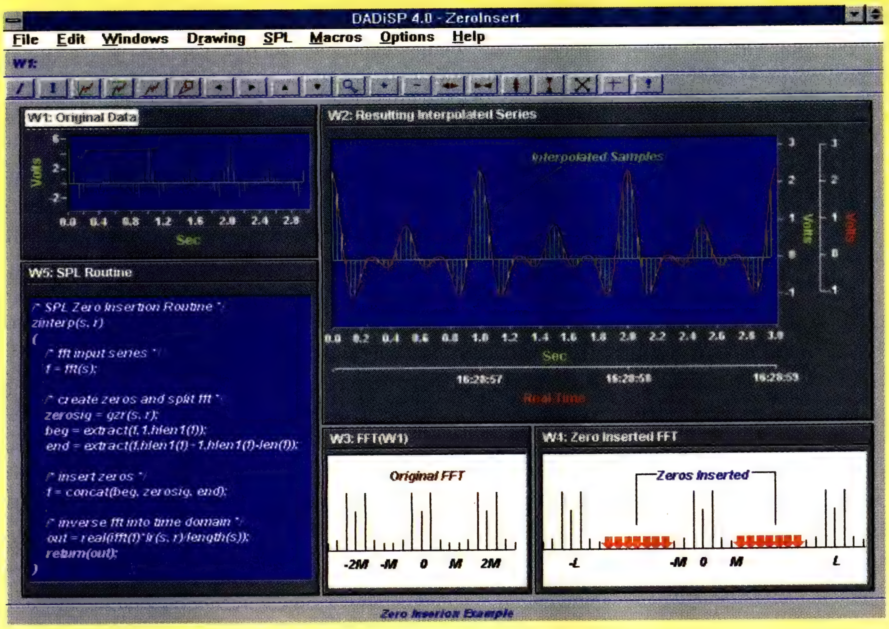
IN CASE YOU MISSED IT!

Here's what **they*** said about DADiSP 4.0

A streamlined user interface that fully conforms to Windows is the first obvious feature of a long-awaited upgrade to DADiSP, a graphical analysis program from DSP Development Corp. that's designed for the needs of scientists and engineers.



```
/* SPL Zero Insertion Routine */
zinterp(s, r)
{
  /* fft input series */
  f = fft(s);

  /* create zeros and split fft */
  zerosig = gzr(s, r);
  beg = extract(f, 1, hlen1(f));
  end = extract(f, hlen1(f)+1, hlen1(f)-len(f));

  /* insert zeros */
  f = concat(beg, zerosig, end);

  /* inverse fft into time domain */
  out = real(ifft(f)*lr(s, r)/length(s));
  return(out);
}
```

A major overhaul of the user interface, the introduction of an integrated programming language and new option modules highlight Ver. 4.0 of DADiSP...

Besides adopting a complete Windows look and feel, the overall interface scheme has gained a more streamlined look... [W]ith the flattened hierarchy on this upgrade, the software always starts up in a worksheet; indeed, when loaded, the software returns to the setup that was on the screen when the user last exited the program. Although you don't have to go through a hierarchy, the package still maintains labbooks, datasets and worksheets to provide a simple method of organizing large complex datafiles and projects.

As part of the Windows implementation, Ver. 4.0 adds support for DDE as a client or server either with functions at the command line or with Copy/ Paste Link for the pulldown menu. It performs both warm and hot DDE links with either ASCII or binary datatypes...

Ver. 4.0 also gives users the ability to define their own operations and functions to a far greater extent than the macros found in the previous version. Specifically, the upgrade marks the introduction of a programming language called SPL (series processing language). Modeled on C, it provides all the expected facilities including user-defined functions, looping and iteration, conditional statements, array references and variables. Variables can be global to a session or local to a function.

An interesting feature is the hot variable, which can contain real or complex numbers, strings, data series and matrices. A hot variable links a formula to a variable so that when a dependent element of a formula changes, the hot variable automatically reevaluates. For example, the SPL code fragment:

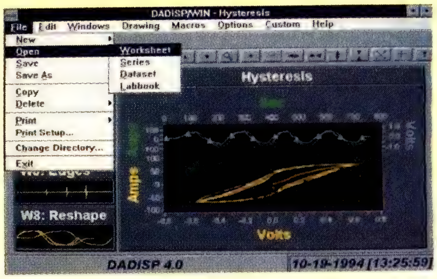
```
size := 10
W2: Movavg(W1, size)
```

performs a 10-point moving average on the waveform in Window 1 and displays the results in Window 2. The := operator establishes the hot variable. You can explore the effects of changing the moving-average length simply by reassigning size := 20 so that W2 automatically updates and shows a plot based on that new parameter.

Also improved is the package's hardcopy facility. Plot titles, legends, multiple scales, selectable fonts and a Preview mode help users produce publication-quality output...

[T]wo more modules... address advanced DSP and control applications. The AdvDSP module performs Chirp-Z transforms, N-point FFTs independent of series length and zoom FFTs. It also handles multiple forms of PSD estimation (classical, autoregressive parametric, moving-average parametric, autoregressive moving-average parametric), transfer-function estimates, Cepstrum analysis and digital interpolation. The controls module allows you to execute command line or pulldown menus, and it addresses the design, analysis and simulation of digital and continuous open- and closed-loop controllers for linear single-input/single-output dynamic systems. Among its algorithms are those that handle PID loops as well as lead and lag controllers.

* Personal Engineering & Instrumentation News 1/95



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8A switcher powers high-performance µPs

CHESTER SIMPSON, NATIONAL SEMICONDUCTOR, SANTA CLARA, CA, (408) 721-7501.

The circuit in **Fig 1** delivers 8A for driving as many as two of today's high-performance, high-speed µPs. You can also optimize the design for lower current by changing a few components. Most systems use a low-current 12V bias supply and a poorly regulated high-current 5V to power the logic. However, the µP requires 3.3V for its main power voltage. Thus, an efficient dc/dc converter that can convert 5 to 3.3V and provide a tightly regulated output voltage is necessary. The primary design objectives for this circuit were minimizing cost, eliminating the need for heat sinks, and providing short-circuit protection to maximize reliability.

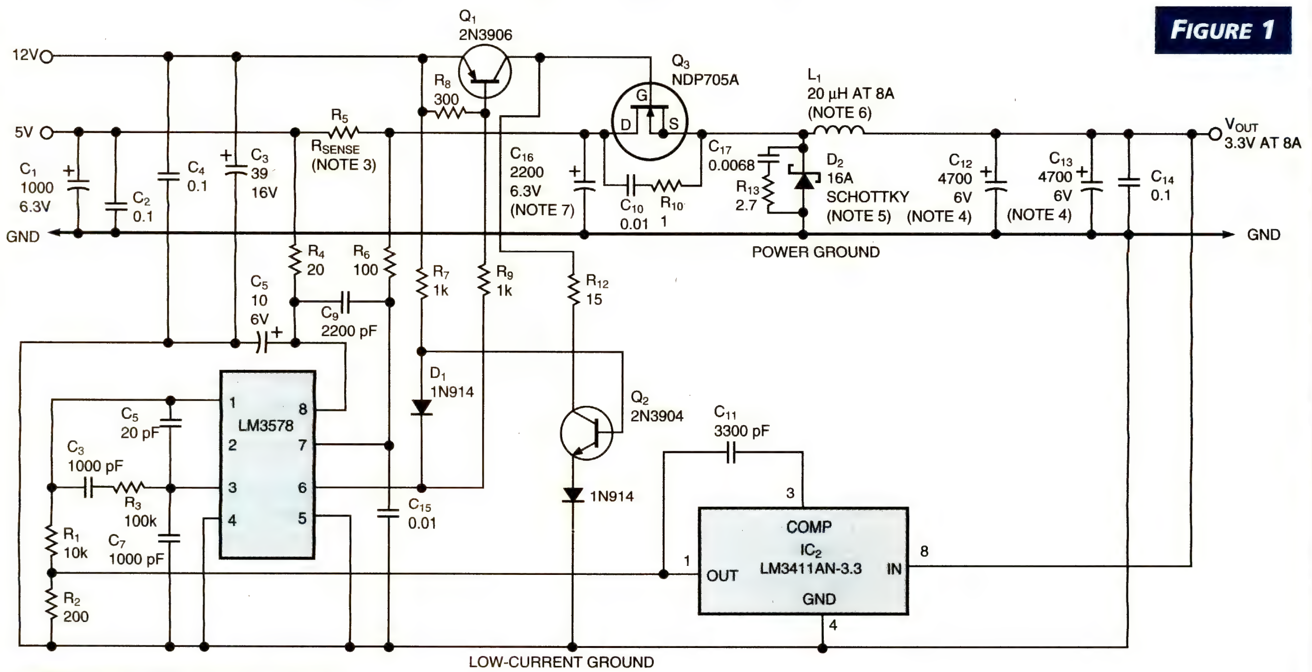
A step-down (buck) regulator that operates at 80 kHz provides the 3.3V/8A output. IC_1 drives the main switching transistor, the N-channel Q_3, through the Q_1 and Q_2 gate-drive transistors. Active drive for the gate of Q_3 is necessary to produce very fast switching transitions, which minimize switching losses.

The open-collector output of IC_1's PWM chip controls Q_1 and Q_2. When pin 6 pulls low, Q_1 turns on through R_9, and Q_2 turns off, because D_1 holds Q_2's base high. This action pulls Q_3's FET switch up to 12V, which turns on Q_3. When pin 6 of IC_1 is high, R_7 turns on Q_2, and R_8 turns off Q_1. In this state, the circuit pulls Q_3's gate to ground, which turns it off. Q_3, catch diode D_2, L_1, C_{12}, and C_{13} provide a dc output capable of sourcing 8A of load current.

Note that you can use an 8A diode for D_2 with only a slight increase in power dissipation in this device. Also, you can use a single 4700-µF output capacitor at the regulator output if output ripple and transient response are not critical.

IC_2, a precision reference whose setpoint voltage is 3.3V±0.5%, provides feedback and voltage control. When the regulator output reaches 3.3V, IC_2 sources current through R_2 to ground, providing feedback to the input of IC_1 and holding the regulator output at 3.3V.

IC_1 and sense resistor R_5 easily implement overcurrent protection. When the voltage drop across R_5 exceeds 110 mV, IC_1 activates its built-in pulse-by-pulse control, which limits the output current. R_5 consists of a piece of AWG 17 resistance wire (type MWS-294: MWS Industries, West Lake, CA, (818) 991-8553) with an effective length of 1.5 in. You can also build R_5 using the same length and gauge of manganin wire.



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTANCE VALUES ARE IN OHMS, 5% TOLERANCE.
2. ALL CAPACITANCE VALUES ARE IN µF.
3. MAKE R_5 FROM AWG 17 RESISTANCE WIRE, EFFECTIVE LENGTH=1.5 IN. (WIRE TYPE MWS INDUSTRIES P/N MWS-294).
4. FOR C_{13}, USE PANASONIC ECA-OJFQ472 OR SIMILAR.
5. FOR D_2, USE IR PART MBR1645-ND OR SIMILAR.
6. L_1=23 TURNS OF AWG 18 COPPER WIRE ON MICROMETALS T68-52A CORE.
7. FOR C_{16}, USE PANASONIC ECA-OJFQ222 OR SIMILAR.

The primary design objectives for this 5 to 3.3V, 8A dc/dc converter were to minimize cost, eliminate the need for heat sinks, and provide short-circuit protection to maximize reliability.

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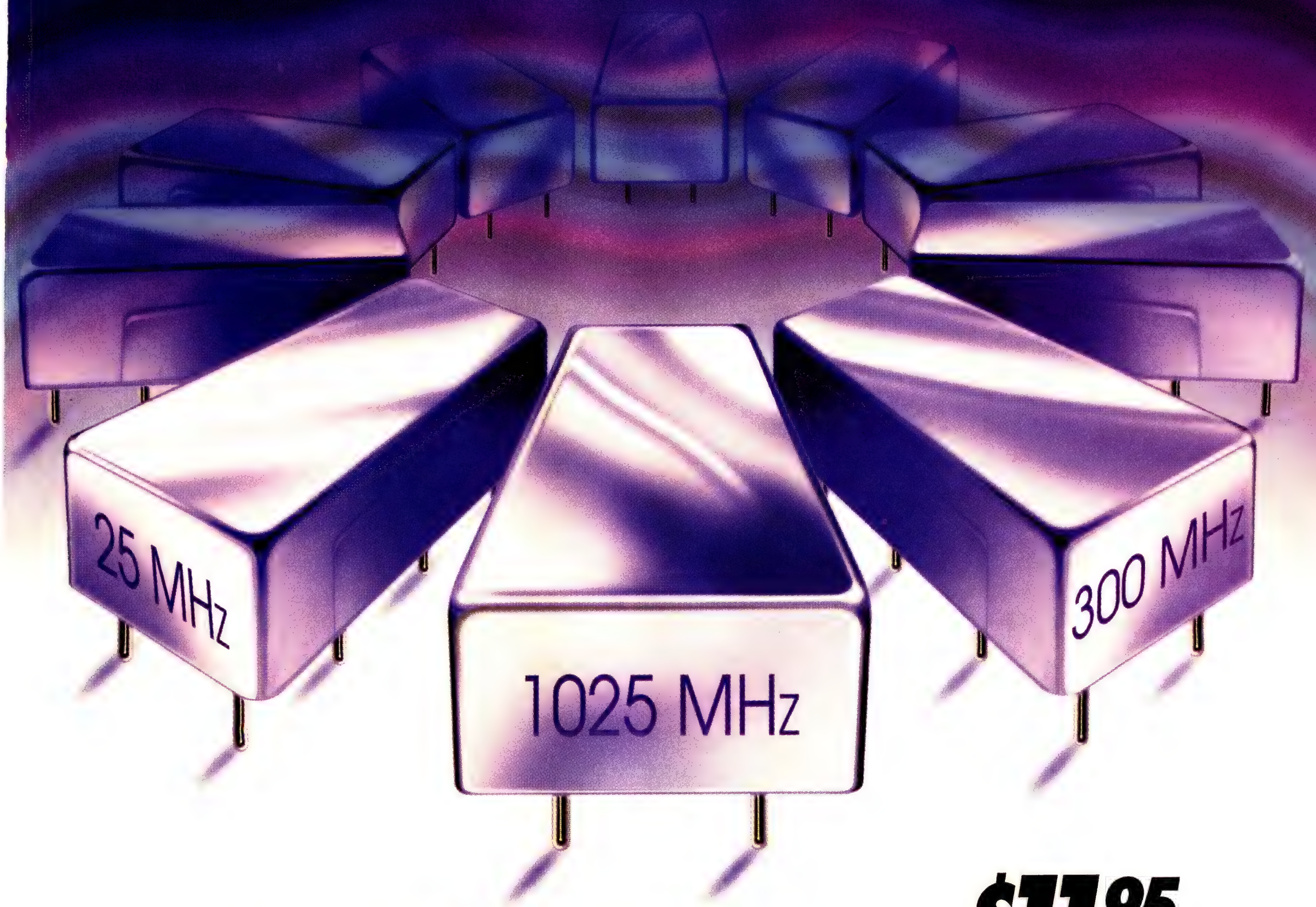

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POS-75	37.5-75	-110	-27	17	11.95
POS-100	50-100	-107	-23	18	11.95
POS-150	75-150	-103	-23	18	11.95
POS-200	100-200	-102	-24	18	11.95
POS-300	150-280	-100	-30	18	13.95
POS-400	200-380	-98	-28	18	13.95
POS-535	300-525	-93	-26	18	13.95
POS-765	485-765	-85	-21	22	14.95
POS-1025	685-1025	-84	-23	22	16.95

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CIRCLE NO. 162

C_{16} must sit very near the drain of Q_3, and C_{16}'s equivalent series resistance (ESR) is critical. Do not substitute a capacitor with higher ESR. The same warning applies to C_{12} and C_{13}: Take care to check ESR specs if you use a substitute.

R_1, R_3, C_3, and C_6 set the loop compensation of IC_1; C_7 sets the oscillator frequency. C_7 should be a good quality ceramic capacitor. C_1, C_2, C_4, and C_8 are necessary for input bypassing, and they reduce the amount of switching noise the circuit conducts onto the input lines. A snubber consisting of R_{10} and C_{10} is necessary to eliminate high-frequency ringing when Q_3 switches off. These components must be located as close as possible to Q_3. R_{13} and C_{17} perform the same function for D_2.

Bench testing indicates the following circuit performance. For V_{IN}=5V, efficiency was 88% for a load current of 4A and 84% for a load current of 8.2A. For V_{IN}=5V and I_{LOAD}=8.2A, noise was 15-mV p-p and 5.5-mV rms using an HP34401A meter. The switcher stayed in regulation with no changes in the output voltage (1-mV measurement accuracy) when the load varied from 0.1 to 8A and when the input voltage varied from 4.5 to 5.5V. With no heat sinks or airflow, the temperature of Q_3 was 70°C and of D_2 was 50°C, when operating at 8.2A continuous load current.

All high-current switchers are sensitive to board layout; take care when designing the pc board. You'll obtain the best results by using a multilayer board, so you can dedicate a single layer to ground plane. You should tie the "power" components (C_1, C_2, C_{16}, D_2, C_{12}, C_{13}, C_{14}) directly to this ground plane and group these components so that the connection paths are as short as possible. You should connect the low-current ground, as **Fig 1** shows, and *then tie it* to the power ground at a single point near C_{13}. Finally, all traces in the switching power path (R_5, Q_3, and L_1) must be as short as possible. (DI #1688) EDN

Ed note: Contact author for a sample of the two-sided pc-board layout he used to implement this design.

To Vote For This Design, Circle No. 320

Battery monitor draws 8 µA or less

Arthur W Du Rea Jr, Science Applications International Corp, Oak Ridge, TN

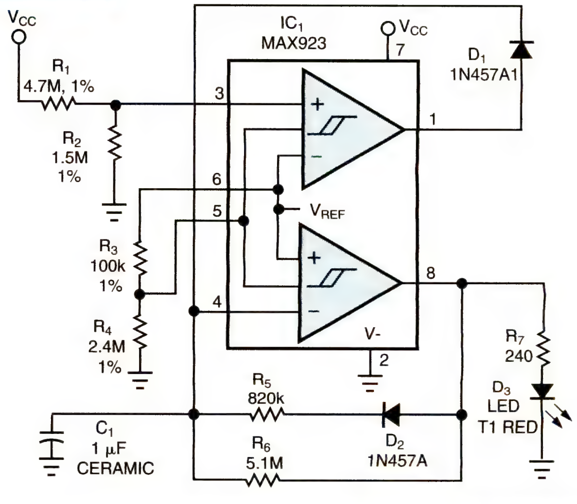
The battery monitor in **Fig 1** nominally draws 5 µA during normal operation and flashes an alarm indicator when the battery voltage drops below a critical value. The alarm-state current depends on the desired indicator brightness, but you can easily make the current average less than 500 µA. This monitor was developed as a change-battery warning in a digital panel meter with a battery life measured in years.

The circuit uses the unique features of a dual comparator and reference, IC_1, to construct an input low-voltage detector to control an RC LED flasher, D_3. The design uses the MAX923 as opposed to the MAX933 because of the 923's 1% on-chip reference. The components in **Fig 1** are for use with a two-cell lithium supply that blinks the alarm LED for 25 msec twice per second when the battery voltage drops below 4.7V. You can adjust the component values for circuit operation over a range of 2.7 to 11V, which are the operating limits of IC_1.

Divider R_1/R_2 sets the alarm indication threshold. The low-going threshold at the comparator input is nominally equal to V_{REF} (1.182V) minus $V_{HYSTERESIS}$ (50 mV max). Divider R_3/R_4 sets the hysteresis for both comparator sections. The values in **Fig 1** set the comparator thresholds approximately 50 mV above and below the reference voltage.

R_5 and D_2 shorten the LED's on time to significantly reduce the average current drain during the alarm state. Removing these components results in approximately symmetrical LED on and off times as set by R_6 and C_1. R_7 sets the LED on current up to a maximum of 17 mA. D_1, D_2, and C_1 must be very low-leakage devices. The 1N457A has a leakage of only 25 nA. C_1 should be a high-quality multilayer ceramic capacitor.

FIGURE 1



This battery monitor nominally draws 5 µA *during* normal operation and flashes an alarm indicator when the battery voltage drops below a critical value.

The component count for this circuit is somewhat high, but the advantage of low-idle current resulting in extended battery life was the determining factor for a particularly power-critical application. (DI #1685) EDN

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Mixed-Tech	Combines chip-and-wire with surface mount	Maximum flexibility
Electro-Optic	Combines chip-and-wire with fiber alignment to 0.25µM and >80% coupling	Minimizes interconnect parasitics between active circuits and electro-optic components
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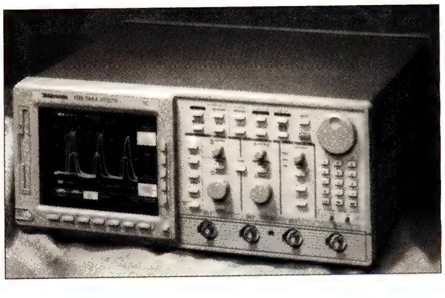

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CIRCLE NO. 157

Timer controls DSP-filter frequency resolution

D HAYDEN, TEMPO RESEARCH, VISTA, CA

To implement low-frequency digital filters, you can use low-power microcontrollers instead of dedicated DSP ICs. However, using 8-bit or even 16-bit math can quickly lead to significant filter dynamic-range errors and to complicated routines for precise digital-filter coefficients. By using a μC's 8-bit timer to set the sampling rate for a digital filter's data processing, you can obtain finer frequency resolution while using simple math routines.

The circuit in **Fig 1** uses a PIC16C71 μC that has an internal 8-bit ADC and an 8-bit timer. The circuit requirement is to provide lowpass filtering over a range of 0.85 to 1.25 Hz for compensating a variable-frequency mechanical system. This application placed other demands on the μC, including terminal software for factory calibration and data mapping and linearization of the output control. The circuit clocks the μC at 62.5 kHz, drawing very low power and giving the internal 8-bit timer a resolution of 64 μsec. By controlling the data sampling rate and using math routines comprising data shifts and additions, the filter the following equation describes yields the lowpass response in **Table 1**:

TABLE 1—LOWPASS FREQUENCY RESPONSE

$T_{SAMPLING}$ (sec)	F_C (Hz)
0.0075	1.37
0.0080	1.28
0.0085	1.21
0.0090	1.14
0.0095	1.08
0.0100	1.03
0.0105	0.978
0.0110	0.933
0.0115	0.893
0.0120	0.856
0.0125	0.822

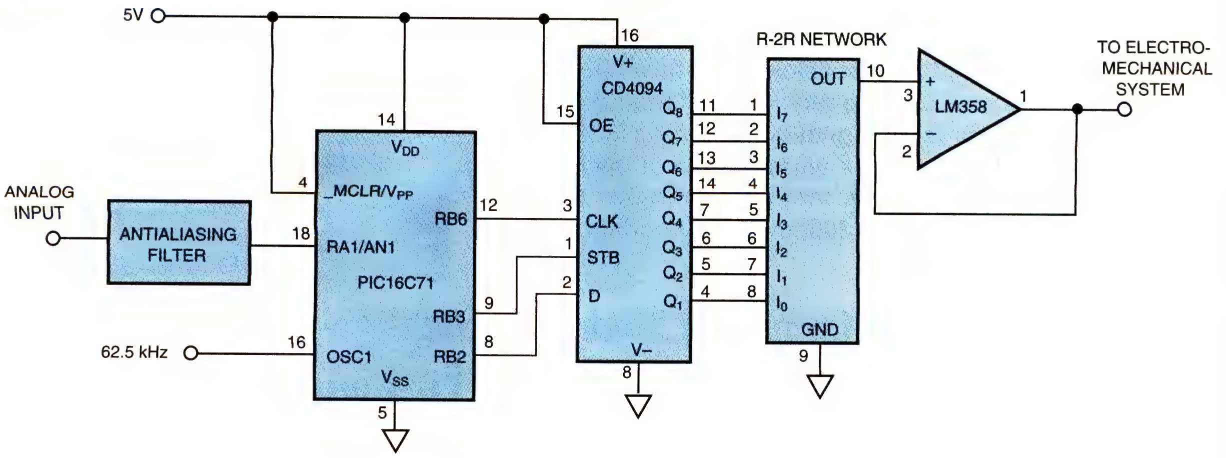
$$y(n)={}^{1}\!/_{16}x(n)+{}^{15}\!/_{16}y(n-1).$$

In contrast, changing the filter coefficients from $^1/_{16}$ and $^{15}/_{16}$ to $^1/_{32}$ and $^{31}/_{32}$, respectively, changes the cutoff frequency from 1.03 Hz to 0.505 Hz. This frequency change is equivalent to a change of 51% at a $T_{SAMPLING}$ equal to 0.00100 sec. Also, changing the coefficients produces smaller resultants, which ultimately reduces the filter's dynamic range. Alternatively, using the original coefficients and changing the sampling period to 0.010064 sec (one timer clock at 62.5 kHz) changes the cutoff frequency from 1.027 to 1.021 Hz, which is a change of only 0.6%. This change provides much more frequency resolution without sacrificing signal dynamic range.

Fig 1 includes an antialiasing filter before the ADC to provide the proper attenuation for high-frequency signals relative to the slowest sampling of the ADC, and a resistor-ladder DAC for the control output. The ZIPfile attached to **EDN BBS /DI_SIG #1684** contains an assembly program for the PIC16C71 μC. The program's excellent documentation should allow you to roll the program over to another μC easily. (DI #1684)

To Vote For This Design, Circle No. 322

FIGURE 1



To obtain finer frequency resolution than that produced by changing filter coefficients, this circuit uses the PIC16C71 μP's internal timer to set a digital filter's data-processing sampling rate.

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The winning Design Idea for the September 29, 1994, issue is entitled "PC acts as RS-232C protocol analyzer," submitted by J S Holmes, Boehringer Mannheim, (Indianapolis, IN).

LINEAR TECHNOLOGY

DESIGN NOTES

A Precision Wideband Current Probe for LCD Backlight Measurement – Design Note 101

Jim Williams

Evaluation and optimization of Cold Cathode Fluorescent Lamp (CCFL) performance requires highly accurate AC current measurement. CCFLs, used to backlight LCD displays, typically operate at 30kHz to 70kHz with measurable harmonic content into the low MHz region[1]. Accurate determination of RMS operating current is important for electrical and emissivity efficiency computations and to ensure long lamp life. Additionally, it is desirable to be able to perform current measurements in the presence of high common-mode voltage (>$1000V_{RMS}$). This capability allows investigation and quantification of display and wiring induced losses, regardless of their origins in the lamp drive circuitry.

Current Probe Circuitry

Figure 1's circuitry meets the discussed requirements. It signal conditions a commercially available "clip-on" current probe with a precision amplifier to provide 1% measurement accuracy to 10MHz. The "clip-on" probe provides convenience, even in the presence of the high common voltages noted. The current probe biases A1, operating at a gain of about 3.75. No impedance matching is required due to the probe's low output impedance termination. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about 200. The individual amplifiers avoid any possible crosstalk-based error that could be introduced by a monolithic quad amplifier. D1 and Rx are selected for polarity and value to trim overall amplifier offset. The 100Ω trimmer sets gain, fixing the scale factor. The output drives a thermally-based, wideband RMS voltmeter. In practice, the circuit is built into a 2.25" × 1" × 1" enclosure which is *directly* connected, via BNC hardware, to the voltmeter. No cable is used. The result is a "clip-on" current probe with 1% accuracy over a 20kHz to 10MHz bandwidth. Figure 2 shows response for the probe-amplifier as measured on a Hewlett-Packard HP-4195A network analyzer.

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[1] Williams, Jim, "Techniques for 92% Efficient LCD Illumination." Linear Technology Corporation AN55, August 1993.

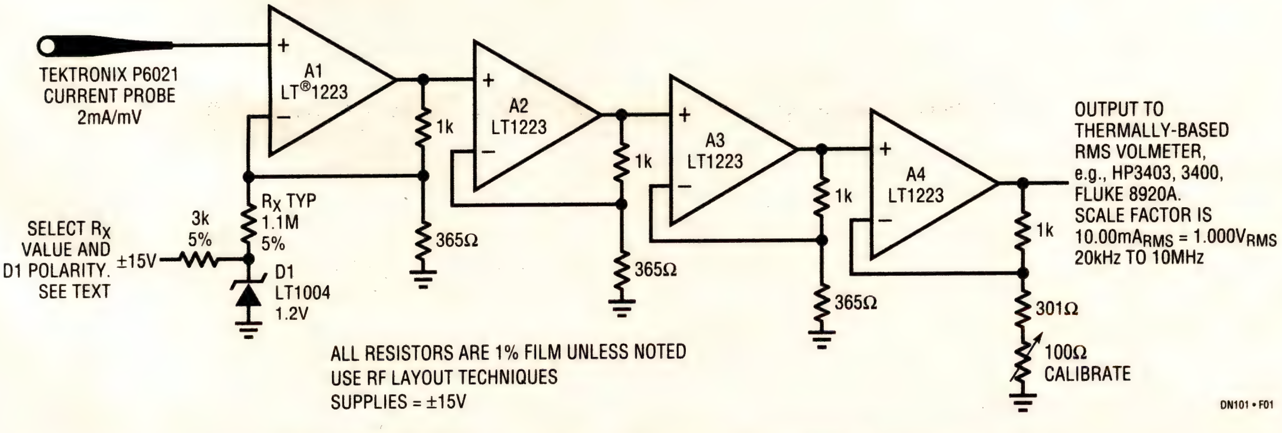

Figure 1. Precision "Clip-On" Current Probe for CCFL Measurements Maintains 1% Accuracy Over 20kHz to 10MHz Bandwith

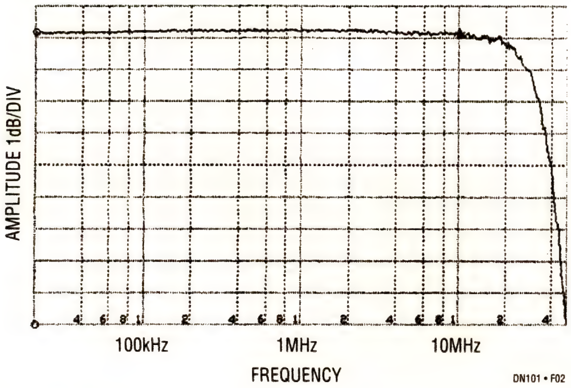

Figure 2. Amplitude vs Frequency Output of HP4195A Network Analyzer. Current Probe-Amplifier Maintains 1% (0.1dB) Error Bandwidth from 20kHz to 10MHz. Small Aberrations Between 10MHz and 20MHz Are Test Fixture Related

Current Calibrator

Figure 3's circuit, a current calibrator, permits calibration of the probe-amplifier and can be used to periodically check probe accuracy. A1 and A2 form a Wein bridge oscillator. Oscillator output is rectified by A4 and A5 and compared to a DC reference at A3. A3's output controls Q1, closing an amplitude stabilization loop. The stabilized amplitude is terminated into a 100Ω, 0.1% resistor to provide a precise 10.00mA, 60kHz current through the series current loop. Trimming is performed by altering the nominal 15k resistor for exactly 1.000V_{RMS} across the 100Ω unit.

In use, this current probe has shown 0.2% baseline stability with 1% absolute accuracy over one year's time. The sole maintenance requirement for preserving accuracy is to keep the current probe jaws clean and avoid rough or abrupt handling of the probe[2].

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[2] Private Communication. Tektronix, Inc.

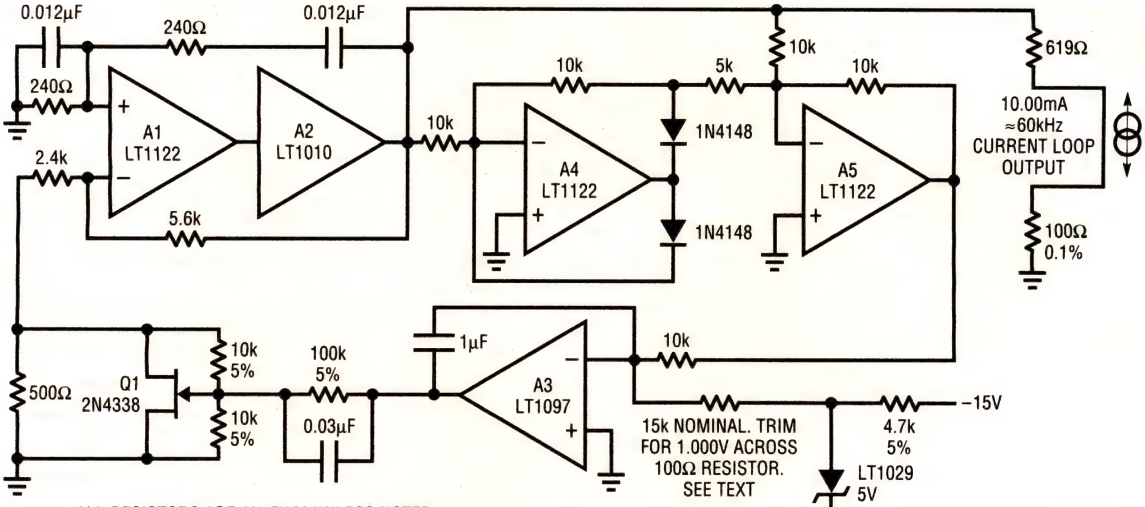

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Figure 3. Current Calibrator for Probe Trimming and Accuracy Checks. Stabilized Oscillator Forces 10.00mA Through Output Current Loop at 60kHz

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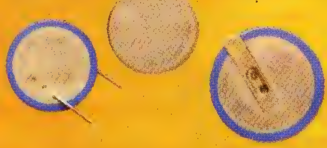

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CIRCLE NO. 210

Finding the keys to flyback power supplies produces efficient design

BROOKS R LEMAN, POWER INTEGRATIONS INC

Many power-supply designers lack a good understanding of flyback-transformer power supplies. The reason is that energy delivered to the load stores in the transformer core itself and not in a separate inductor. A quick tutorial on flyback-power-supply design may help clear out some of the cobwebs.

Power-transformer design is the biggest stumbling block in developing switching power supplies. Even more intimidating is developing flyback power supplies, because designers don't use flyback transformers like normal transformers. Energy stores in the core, and the core must be gapped. Current flows in either the primary or secondary winding but never in both windings simultaneously.

Designers use the flyback topology because flyback power supplies require the fewest components. At lower power levels, total component cost is less than with other techniques. However, between 75 and 100W, increasing voltage and current stresses cause flyback-component cost to increase significantly. At these high power levels, topologies with lower voltage- and current-stress levels (such as the forward converter) are more cost-effective, even with higher component counts.

Flyback-transformer design, which requires iteration through a set of design equations, is not difficult. Simple spreadsheet iteration reduces design time to less than 10 minutes for a transformer that usually works the first time. This method, which works for both continuous- and discontinuous-mode designs, has three distinct steps:

- Identify and estimate the set of independent variables that depend on the application, transformer core, and TOPSwitch.
- Identify and calculate dependent parameters.
- Iterate specified independent variables until specified dependent parameters fall within defined limits for a practical flyback transformer.

An Excel spreadsheet (**Table 1**) automates the transformer design method this article details. Depending on the application, the **table** lists independent variables, beginning with output power and ending at the input filter capacitor. Transformer-core and construction variables are the next listings. Depending on the TOPSwitch (or other PWM circuit), variables include switching frequency, duty cycle, peak primary current, and MOSFET voltage drop.

For a given application and transformer core, calculate or estimate 19 of 22 variables, which will remain fixed during iteration. Only three variables, number of secondary turns, N_S, peak primary current, I_P, and number of primary winding layers, L, will change during the iteration process. Dependent parameters (also in the **table**) divide into four groups: dc-input voltage, primary-current waveform shape, transformer design, and voltage stress.

During iteration, only four of the 23 dependent parameters are compared to limits. Check primary-ripple to peak-current ratio, K_{RP}, maximum flux density, B_M, gap length, L_G, and primary current capacity, CMA, with each iteration until all four parameters are within specified limits. The remaining 19 dependent parameters are either intermediate calculations or parameters the manufacturer uses for construction. You need to gain an understanding of the shape of the primary and secondary current waveforms in both continuous and discontinuous operation before beginning transformer design.

AC mains drives power supply

Fig 1 shows a typical flyback power supply using the PWR-TOP202 TOPSwitch from Power Integrations Inc (Mountain View, CA, (415) 960-3572). The TOPSwitch combines an integrated high-voltage MOSFET switch with a complete switching power-supply controller and protection circuitry in a single device. In the **figure**, the power-supply circuit operates from 85 to 265V ac and delivers 15W at 7.5V output. BR1 and C1 (C_{IN}) rectify and filter ac power to create the high dc voltage applied to the primary winding of T1. The high-voltage MOSFET Q1 within the TOPSwitch drives the other side of the transformer primary. D1 and VR1 clamp voltage spikes that transformer leakage inductance causes.

D2, C2, L1, and C3 rectify and filter the power secondary.

D3 and C4, which rectify and filter the bias winding, provide the TOPSwitch bias voltage. EMI-filter components L2, C6, C7, and C8 reduce conducted-emission currents. Bypass-capacitor C5 filters internal MOSFET-gate charge-current spikes and compensates the control loop. Regulation is achieved when the output voltage rises sufficiently above zener diode voltage (VR2) to cause optocoupler photodiode current to flow. Optocoupler-phototransistor current flows into the TOPSwitch control pin to control the duty cycle and output voltage directly. Together with VR2 series impedances and the TOPSwitch, R1 determines the control-loop dc gain. R2 and VR2 provide a slight preload to improve regulation at light loads.

Figs 2a and **b** show typical voltage and current waveforms taken from the same power supply, delivering 15W from 110V-ac input voltage but with different flyback-transformer primary inductances. Q1 turns on and effectively applies the dc input voltage across the transformer winding with the "dot" side at lower potential than the "no-dot" side. Primary current, I_{PRI}, increases linearly with a rate of change (dI/dt) that varies directly with dc input voltage and inversely with primary inductance. Ripple current, I_R, is defined as the incremental linear current rise (dI) over the entire Q1 on time (t_{ON}).

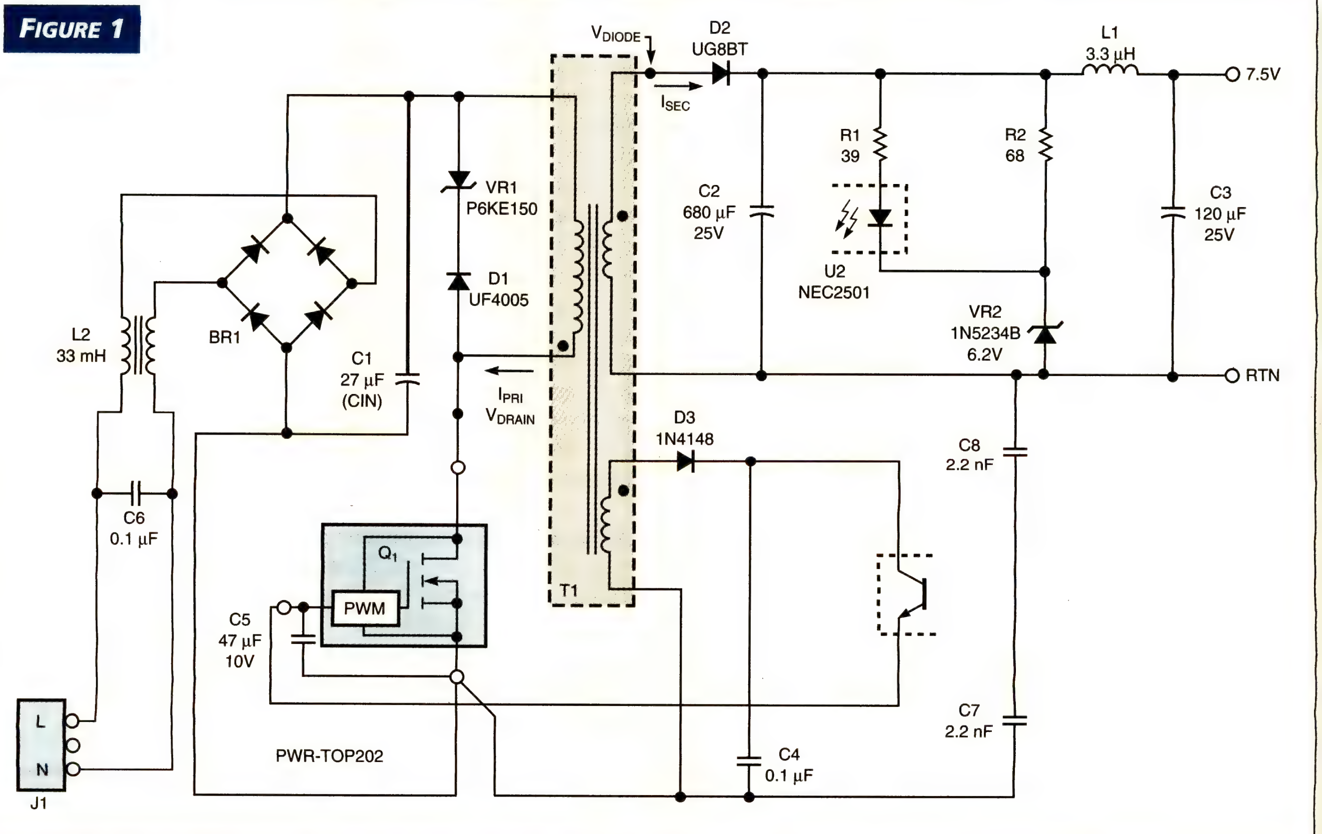
Peak primary current, I_P, is the final value that occurs as Q1 turns off. Energy proportional to the square of peak current, I_P, stores by magnetic field in the transformer core as if the primary winding were a simple inductor. The secondary winding carries a reflected voltage proportional to primary voltage by turns ratio with the same dot polarity. While Q1 is on, output-diode D2 and bias-diode D3 reverse-bias and prevent secondary current flow. When Q1 turns off, the decreasing magnetic field induces an abrupt voltage reversal on all transformer windings, such that the dot side is now at a higher potential than the no-dot side.

Diodes D2 and D3 become forward-biased, and secondary current rises quickly to a peak value (proportional by the inverse turns ratio to primary peak current, I_P). Primary current immediately drops to zero. The MOSFET drain voltage quickly rises to a voltage equal to the sum of the dc input voltage and reflected output voltage. Secondary winding current now linearly decreases at a rate that varies directly with output voltage and inversely with secondary inductance. Duty cycle, D, is defined as the ratio of Q1 on time, t_{ON}, to the switching period, T. You can also calculate D from t_{ON} and switching frequency f_s as shown:

$$D = \frac{t_{ON}}{T} = t_{ON} \times f_s.$$

Fig 2a shows MOSFET and diode triangular-current waveforms, which define "discontinuous" mode of operation resulting from low primary inductance. The secondary current linearly decreases to zero before MOSFET Q1 turns on

FIGURE 1



This flyback transformer operates from a 110V-ac mains and delivers 7.5V dc at 15W.

again. The stored energy is completely delivered to the load. The MOSFET drain voltage, V_{DRAIN}, relaxes and rings back toward the dc bus voltage when no current is flowing in either primary or secondary.

Fig 2b shows trapezoidal current waveforms, which define "continuous" mode of operation resulting from high primary inductance. Secondary current is still flowing when MOSFET Q1 turns on at the beginning of the next cycle. The stored energy isn't completely delivered to the load. Energy (and nonzero magnetic field) remains in the core when MOSFET Q1 turns on again, causing the initial step in MOSFET current. Note that MOSFET drain voltage, V_{DRAIN}, stays at a high value equal to the sum of the dc input voltage, V_{DC}, and reflected output voltage, V_{OR}, until Q1 turns on again.

Current never flows in the primary and secondary winding simultaneously; neither primary nor secondary current is actually continuous. In flyback power supplies, continuous/discontinuous mode refers to magnetic-field continuity in the transformer core over one complete switching cycle. (The flyback power supply is an isolated version of the simple buck-boost converter, where inductor current continuity defines continuous and discontinuous modes.)

Each primary current waveform has a peak value, I_P, a ripple current value, I_R, an average or dc value, I_{AVG}, and an rms value, I_{RMS}. I_P determines the number of primary turns and the core size necessary to prevent transformer saturation; it must also be below the TOPSwitch peak current limit. I_{AVG} is the average or dc primary current as well as the input current, which is proportional to output power. I_{RMS} produces power losses due to winding resistance and MOSFET RDS_{ON}. The ratio, K_{RP}, of ripple, I_R, to peak current, I_P, defines the continuous waveform. K_{RP} also simplifies subsequent calculations, such as I_{RMS}.

Transformers designed for discontinuous operation have a higher peak current and a ripple-to-peak current ratio, K_{RP}, equal to 1. Practical continuous designs have lower peak currents and a ripple-to-peak current ratio, K_{RP}, less than 1, but typically greater than 0.33. K_{RP} is inversely proportional to primary inductance, so a continuous design will

TABLE 1--FLYBACK-TRANSFORMER-DESIGN SPREADSHEET EXAMPLE: ST202 INSULATED WIRE TRANSFORMER CORE: TDKPC30EE22-Z*

ENTER APPLICATION VARIABLES		
PO	15W	Output power
VO	7.5V	Output voltage
VB	12V	Bias voltage
VD	0.4V	Output-winding-diode forward-voltage drop
VDB	0.7V	Bias-winding-diode forward-voltage drop
n	0.8	Efficiency estimate
fL	60 Hz	AC-mains frequency
VACMAX	265V	Maximum ac input voltage
VACMIN	85V	Minimum ac input voltage
tC	2 µsec	Bridge-rectifier conduction-time estimate
CIN	33 µF	Input-filter capacitor
ENTER TRANSFORMER-CORE/CONSTRUCTION VARIABLES		
AE	0.41 cm^2	Core effective cross-sectional area
LE	3.96 cm	Core effective path length
AL	2400 nH/T^2	Ungapped effective inductance
BW	0.332 in.	Bobbin physical-winding width
M	0 in.	Safety-margin width
L	2	Number of primary layers
NS	6	Number of secondary turns
ENTER PWM VARIABLES		
fS	100000 Hz	Switching frequency
D	0.5	Duty cycle at minimum dc input voltage (V dc)
IP	0.6812A	Peak primary current
VDS	3V	Drain-to-source voltage (MOSFET on)
DC INPUT VOLTAGE PARAMETERS		
VMAX	375V	Maximum dc input voltage
VMIN	85V	Minimum dc input voltage
PRIMARY-CURRENT WAVEFORM-SHAPE PARAMETERS		
IAVG	0.2282A	Average primary current
IR	0.4496A	Primary ripple current
KRP	0.66	Ripple-to-peak current ratio (0.33<KRP<1.0)
IRMS	0.3355A	Primary rms current
TRANSFORMER-DESIGN PARAMETERS		
LP	914 µH	Primary inductance
NP	62	Primary number of turns
ALG	235 nH/T^2	Gapped core effective inductance
ur	1845	Relative permeability of ungapped core
BWE	0.664 in.	Effective bobbin width
DIA	11 mils	Primary wire diameter
BM	2433 Gauss	Maximum flux density (2000<BM<2500)
BAC	803 Gauss	AC flux density for core loss curves (0.53 p-p)
LG	7.80 mils	Gap length (2<<LG)
CMA	337 Cmils/A	Primary winding current capacity (200<CMA<500)
ISRMS	3.49A	Secondary rms current
DIASEC	34 mils	Secondary minimum conductor diameter
ODSEC	55 mils	Secondary maximum conductor diameter
NB	10	Bias winding number of turns
VOLTAGE-STRESS PARAMETERS		
VOR	82V	Output-voltage reflected to primary
VDRAIN	457V	Maximum drain voltage (excluding leakage-inductance spike)
VPIV	44V	Output-rectifier maximum peak inverse voltage

*This spreadsheet is available on the EDN Readers' BBS. Phone (617) 558-4241 with modem settings 1200/2400 8, N, 1 (9600 baud=(617) 558-4580). From the Main System Menu enter ss/freeware. Then from the /freeware SIG menu enter rkms914.

have a higher inductance. Continuous-transformer designs have a practical primary-inductance upper limit between five and six times that of a discontinuous design at the same input voltage and output power, which is a result of the difference in peak currents and K_{RP} ratios.

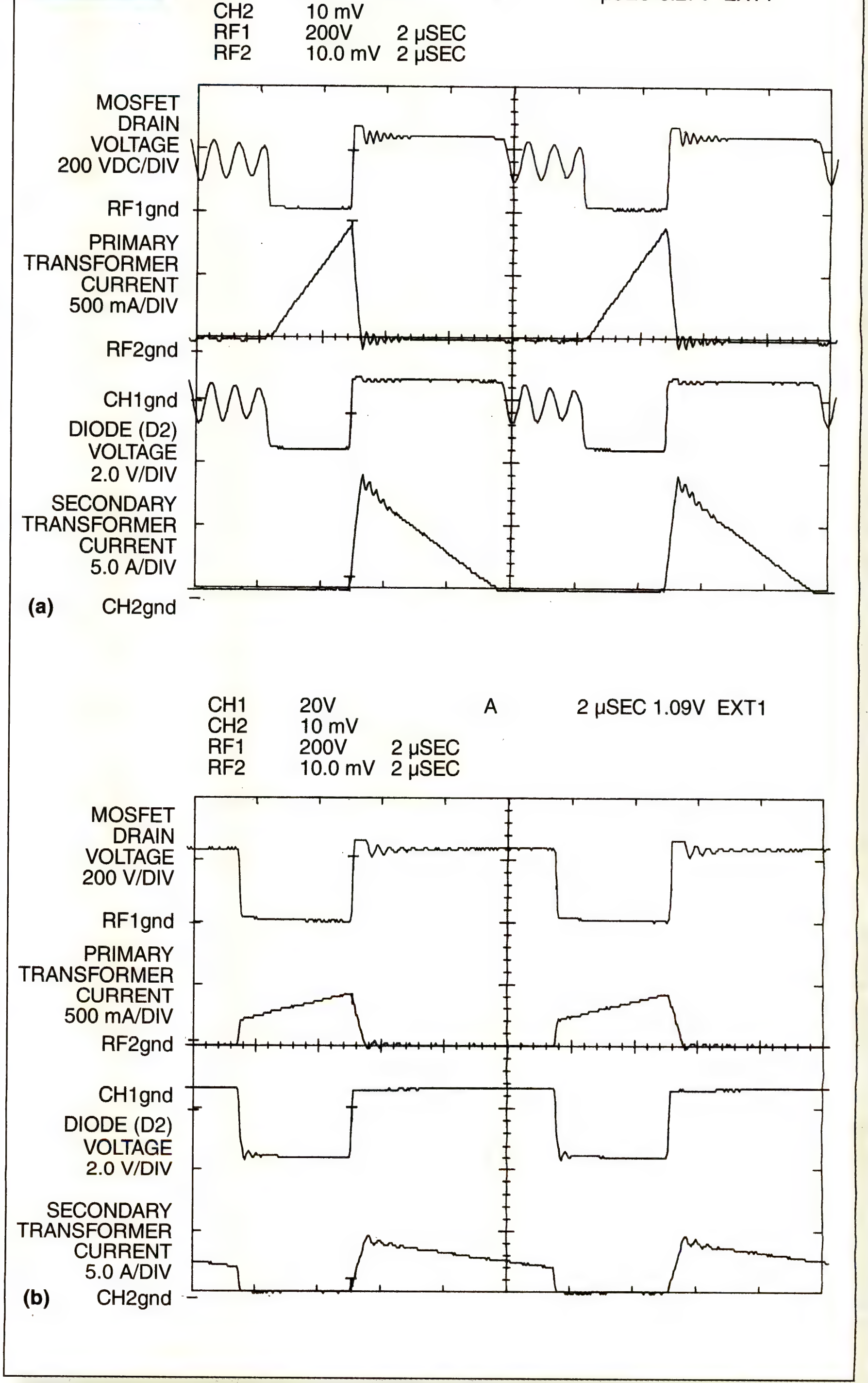
The primary-current waveforms in **Figs 2a** and **b** deliver the same output power and, therefore, must have equal I_{AVG} current. The discontinuous current waveform has a higher peak value and thus must have a higher rms current value. Discontinuous mode requires less inductance and reduces transformer size but, due to higher rms currents, operates with higher losses and lower efficiency. Continuous mode requires higher inductance and larger transformers but offers improved efficiency and lower power losses. The tradeoff between transformer size and power-supply efficiency depends on the packaging and thermal environment in each application.

Feedback control stability

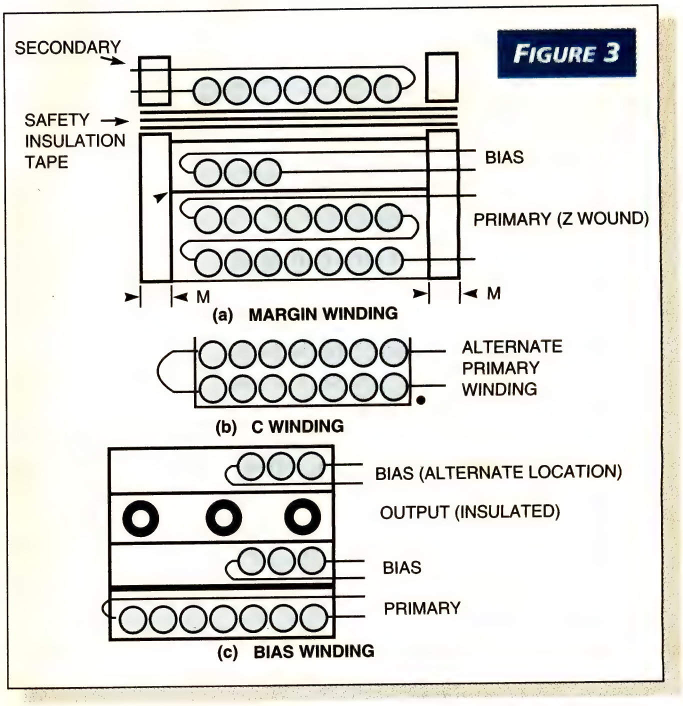
Most designers avoid the continuous mode because the feedback control loop is more difficult to analyze. Discontinuous-mode power supplies can be modeled with a single pole response and are simple to stabilize. In continuous mode, a right half-plane zero and complex pole pair that all shift with duty cycle make analysis difficult. Stabilizing the continuous system is quite straightforward with adequate phase margins over all line and load combinations. You can limit right half-plane zero and complex-pole-pair migration with duty cycle by designing for a maximum duty cycle of 50% at low line and heavy load. Improve phase margins by taking into account the effective power path series resistance and capacitor equivalent series resistance. Crossover bandwidths up to 1 kHz are easy to achieve with phase margins of at least 45°.

Before beginning design work, spend time considering transformer-core, winding, and safety issues. Transformer-core and construction parameters depend on the selected

FIGURE 2



The voltage and current waveforms in (a) are representative of discontinuous operation, which results in low primary inductance. Triangular-current waveforms characterize discontinuous operation, where stored energy is completely delivered to the load. The voltage and current waveforms in (b) are representative of continuous operation, which results in high primary inductance. The secondary current is still flowing when the MOSFET turns on at the beginning of the next cycle, so stored energy isn't completely delivered to the load.



Three methods for transformer winding include margin winding (a), C winding (b), and bias winding (c).

core and winding techniques used in assembly. Physical height and cost are usually most important when selecting cores, which is especially true in ac-mains adapter power supplies that are normally packaged in sealed plastic boxes. Applications allowing at least 0.75 in. of component height can use low-cost EE or EI cores from Magnetics Inc; Japanese-vendors TDK and Tokin; or European-vendors Philips, Siemens, and Thomson. Applications requiring lower profile can benefit from EFD cores available from the European vendors. EER cores offer a large window area, require few turns, and have bobbins available with high pin counts for applications requiring multiple outputs. When space is not a problem, ETD cores are useful in higher power designs. PQ cores are more expensive but take up slightly less pc-board space and require fewer turns than E cores. Safety isolation requirements make pot cores, RM cores, and toroids generally unsuitable for flyback power supplies operating from the ac mains.

Flyback transformers must provide isolation between primary and secondary in accordance with the regulatory agencies of an intended market. For example, information-technology equipment must meet the requirements of IEC950 in Europe and UL1950 in North America. These documents specify distances for creepage and clearance as well as insulation systems used in transformer construction. A 5-mm creepage distance is usually sufficient between primary and secondary (check with appropriate agency and specification). Isolation is usually specified by electric strength and is tested with a voltage of typically 3000V ac applied for 60 sec. Two layers of insulation (basic and supplementary) are appropriate between primary and secondary if each layer exceeds the electric-strength requirement. Use three layers of insulation (reinforced) if all combinations of two layers (out of three total) meet the electric-strength requirement.

Multiple ways to wind a bobbin

Fig 3a shows the margin-winding technique used in most flyback transformers. The margin is usually constructed with layers of tape slit to the width of the desired margin and wrapped in sufficient layers to match the winding height. The margin is generally half the required primary-to-secondary creepage distance (2.5 mm, or 100 mils in this example). To maintain transformer coupling and reduce leakage inductance, cores and bobbins should be large enough that the actual winding width is at least twice the total creepage distance. The primary is wound between the margins. To reduce the risk of interlayer voltage breakdown due to insulation abrasion, improve layer-to-layer insulation, and decrease capacitance, separate the primary layers by at least one layer of UL-listed polyester film tape (3m 1298) cut to fit between the margins. Varnish or epoxy impregnation can also improve layer-to-layer insulation and electric strength but do not reduce capacitance. The bias winding then winds over the primary.

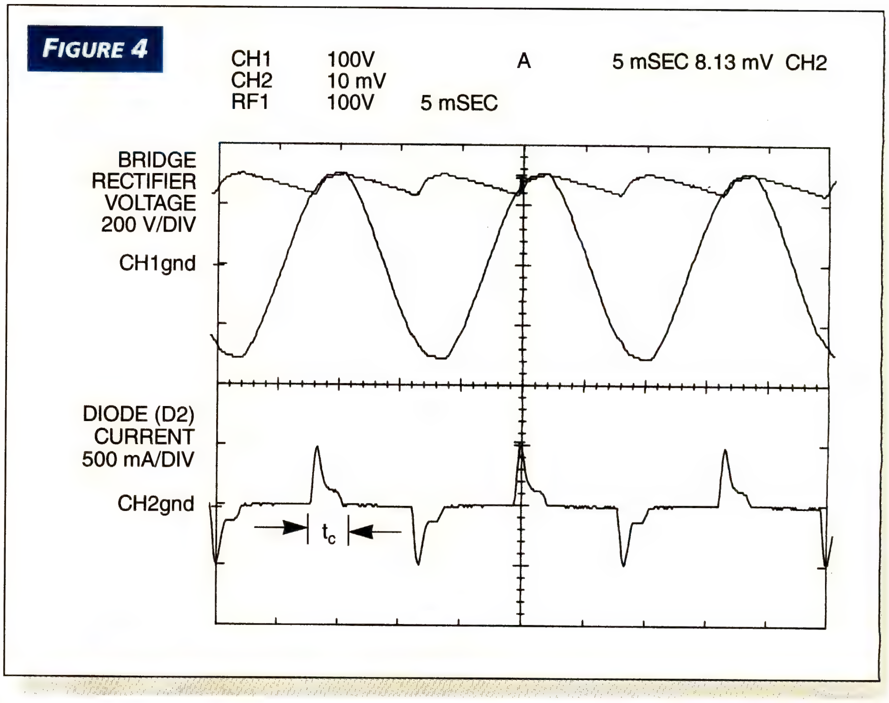
Supplementary or reinforced insulation consisting of two or three layers of UL-rated polyester film tape cut to the full width of the bobbin then wraps over the primary and bias windings. Margins are wound again. The secondary winding is wound between the margins. To secure the windings, add another two or three layers of tape. To meet creepage-distance requirements at lead exits, you may need to use insulation sleeving over the leads of one or all windings. To meet safety-agency requirements, use nylon or Teflon sleeving with a minimum wall thickness of 0.41 mm (16 mils). Consider the core as isolated dead metal, which means the core is conductive but not part of any circuit—and safely insulated from the consumer. The sum of the distance from primary winding (or lead exits) to the core, and the distance from the core to the secondary (or lead exits) must be equal to or greater than required creepage distance.

Figs 3a and b, respectively, show Z and C winding techniques for multiple primary layers. To reduce EMI (common-mode conducted emission currents), the dot side, which connects to the MOSFET, is buried under the second layer for self-shielding. Z winding decreases transformer capacitance, decreases ac MOSFET losses, and improves efficiency but is more difficult and costly to wind. C winding is easier to use and costs less—but at the expense of higher loss and lower efficiency.

Fig 3c shows a new technique using double- or triple-insulated wire on the secondary to eliminate the need for margins . In double-insulated wire, each layer usually meets safety-agency electric-strength requirements. In triple-insulated wire, all three two-layer combinations taken together must meet the electric-strength requirement. Take special care to prevent insulation damage during winding and soldering. This technique reduces transformer size and eliminates the labor cost of adding margins, but it incurs higher material cost and may increase winding costs. The primary winding is wound over the full width of the bobbin flange. If desired, the bias winding can be wound over the primary. To prevent insulated-wire abrasion, use one layer of tape between primary or bias and secondary. The double- or triple-insulated wire is then wound. Add another layer of tape to secure insulated winding.

Fig 3c also shows an alternate position for the bias winding wound directly over the secondary, which improves coupling to the secondary winding and reduces leakage inductance (it improves load regulation in bias-winding feedback circuits). Note that, because the bias winding is a primary circuit, margin-wound transformers must have another layer of supplementary or reinforced insulation between the secondary and alternate bias winding.

FIGURE 4



C_{IN} charges to the peak of the ac input voltage during a short conduction time, t_C. Diode D2 conducts secondary current during this time.

Flyback-power-supply design

To begin a flyback-transformer design, you need to specify three groups of independent variables.

Application variables:
Derive output power, P_O, output voltage, V_O, bias voltage, V_B, ac mains frequency, f_L, and minimum and maximum ac mains voltage, V_{ACMIN} and V_{ACMAX}, respectively, directly from specifications for each application.

Output-rectifier forward-voltage drop, V_D, depends on output voltage. For output voltages lower than 7.5V, use a Schottky diode (V_D is typically 0.4V). For higher output voltage, use of an ultrafast-recovery PN junction diode is normal, and V_D is typically 0.7V. Bias-winding-diode forward-voltage drop (V_{DB}) is also typically 0.7V.

For efficiency (n), start with an estimate based on measurements in similar power supplies or use a value of 0.8 if data is unavailable. For input-filter-capacitor C_{IN}, start with a standard value in microfarads, from two to three times the output power (in watts). For example, 30 to 45 μF is a suitable capacitance range for a 15W supply. A capacitance of 33 μF is the lowest standard value within the range. For bridge-rectifier conduction time, t_C, 2 msec is typical (measure on a similar power supply or set equal to 0 for a conservative first design).

Transformer-core/construction variables:
The following effective parameters are specified by the core and bobbin manufacturer in data sheets: cross-sectional area, A_E (cm^2), path length, L_E (CM), ungapped inductance, A_L (specified in either millihenries/(1000 turns)^2 or nanohenries/turns^2), and physical bobbin-winding width, B_W. Margin-width M, which is determined by the insulation methods and regulatory requirements detailed above, is usually either 0.10 in. or set to 0.

For number of layers, L, one or two layers of primary winding are usually sufficient when switching at 100 kHz or above. Higher layer numbers reduce coupling and increase cost, capacitance, and leakage inductance. Number of secondary turns, N_S, is a key iteration variable. For N_S, one turn per volt of output voltage is a good value with which to begin (for example, start with five turns for a 5V output).

PWM variables:
Switching frequency, f_S, is fixed at 100 kHz for the TOPSwitch. For maximum-duty-cycle D, most flyback power supplies specify a value of 0.5 at the minimum dc input voltage where full-load voltage regulation is required. Under some conditions, for a given TOPSwitch, a higher duty cycle may increase the power level or reduce losses and voltage stress on the output diode. The benefits of higher-duty-cycle operation come at the expense of an increased number of primary turns, as well as higher MOSFET voltage stress and power dissipation.

Primary peak current, I_P, is the other key iteration variable that directly determines current-waveform shape and primary inductance. For universal (85 to 265V-ac) or 100 to 120V-ac input voltage, 50 mA/W of output power is a good starting point for I_P (for example, start with peak current of 500 mA for a 10W output). For 230V-ac input voltage, 25 mA/W of output power is appropriate for peak current, I_P. V_{DS} is the on-state MOSFET voltage taken from the TOPSwitch or MOSFET data sheet at the specified value for I_P.

Now you can calculate the four groups of dependent parameters.

DC-input-voltage parameters:
Maximum dc input voltage is simply the peak value of the highest ac input voltage, VAC_{MAX}, expected in the applica-

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tion. Operation from 265V-ac input results in a maximum dc bus voltage, V_{MAX}, of 375V dc.

$$V_{MAX} = V_{ACMAX} \times \sqrt{2} = 265 \times \sqrt{2} = 375$$

Minimum dc input voltage, V_{MIN}, depends on the ac input voltage, bridge rectifier, and energy-storage capacitor. **Fig 4** shows how C_{IN} charges to the peak of the ac input voltage during a short conduction time, t_C. Because of full-wave rectification, C_{IN} has a ripple voltage at twice the line frequency. C_{IN} must supply the entire average primary current during the discharge time between the peaks of the ac input voltage. Derive minimum dc voltage, V_{MIN}, from the following equation, where P_O is the power-supply output power, n is an estimate of efficiency, f_L is line-voltage frequency, V_{ACMIN} is the minimum ac-mains voltage, C_{IN} is the value of the filter capacitor, and t_C is an estimate for conduction time. As an example, for a 60-Hz, 85V-ac input voltage, 0.8 efficiency, 15W output power, 33-μF input filter capacitance, and 2-msec estimated conduction time, V_{MIN} is 85V dc.

$$V_{MIN} = \sqrt{\left(2 \times V^2_{ACMIN}\right) - \left(\frac{2 \times P_O \times \left(\frac{1}{2 \times f_L} - t_C\right)}{n \times C_{IN}}\right)} = \sqrt{\left(2 \times 85^2\right) - \left(\frac{2 \times 15 \times \left(\frac{1}{2 \times 60} - 2\ \text{msec}\right)}{0.8 \times 33\,\mu F}\right)} = 85V$$

Current-waveform-shape parameters:

Calculate average current from effective primary voltage (the difference between minimum dc input voltage, V_{MIN}, and drain-source voltage V_{DS}), output power, P_O, and efficiency, n:

$$I_{AVG} = \frac{P_0}{n \times (V_{MIN} - V_{DS})}.$$

Calculate ripple current from average current, I_{AVG}, peak primary current, I_P, and maximum duty cycle, D:

$$I_R = 2 \times \left(I_P - \left(\frac{I_{AVG}}{D}\right)\right).$$

Note that ripple-to-peak-current ratio, K_{RP}, is an important dependent variable to watch during iteration. Peak primary current, I_P, varies to keep K_{RP} within the limits of 0.33 (heavy continuous) to 1.0 (discontinuous).

$$K_{RP} = \frac{I_R}{I_P}$$

Calculate rms current, I_{RMS}, from maximum duty cycle, D, peak primary current, I_P, and ripple-to-peak ratio, K_{RP}. You can also calculate I_{RMS} directly from D, I_{PK}, and ripple-current I_R.

$$I_{RMS} = I_{PK} \times \sqrt{D \times \left(\frac{K^2_{RP}}{3} - K_{RP} + 1\right)} = \sqrt{D \times \left(I^2_{PK} - (I_{PK} \times I_R) + \frac{I^2_R}{3}\right)}$$

Calculate transformer-design parameters:

Primary inductance (in microhenries) is a simple function of ripple current, I_R, effective primary voltage, duty-cycle D, and switching frequency, f_S:

$$L_P = 10^6 \times \frac{(V_{MIN} - V_{DS}) \times D}{I_R \times f_s}.$$

The number of primary turns depends on the number of secondary turns, N_S, output voltage, V_O, diode forward-voltage drop, V_D, minimum dc input voltage, V_{MIN}, the MOSFET, V_{DS}, and duty cycle, D:

$$N_P = N_S \times \frac{V_{MIN} - V_{DS}}{V_O + V_D} \times \frac{D}{1-D}.$$

A_{LG} is the effective inductance for the gapped core in nanohenries/turns². Some core vendors offer standard gapped core sets with specified A_{LG}. The transformer manufacturer either procures the gapped core for the given A_{LG} value or grinds the gap to meet the inductance specification in the finished transformer. Also, use A_{LG} to simplify subsequent calculations. Calculate A_{LG} from primary inductance, L_P (in μH), and number of primary turns, N_S.

$$A_{LG} = 1000 \times \frac{L_P}{N^2_P}$$

Calculate relative permeability, μ_r, of the ungapped core to estimate the gap length, L_G. Find μ_r from core parameters A_E (cm), L_E (cm), and ungapped-effective-inductance A_L:

$$u_r = \frac{A_L \times L_E}{0.4 \times \pi \times A_E \times 10}.$$

Effective bobbin width, B_{WE}, takes into account physical bobbin width, B_W, margins M, and number of layers, L:

$$B_{WE} = L \times (B_W - (2 \times M)).$$

Find primary wire diameter, DIA (in mils), from effective bobbin width, B_{WE}, and number of primary turns, N_P:

$$DIA = 1000 \times \frac{B_{WE}}{N_P}.$$

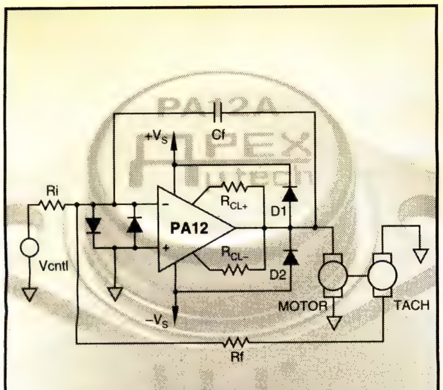
Maximum flux density, B_M, is a dependent iteration variable to be manipulated between the limits of 2000 and 2500 gauss by varying the number of secondary turns, N_S, which directly varies number of primary turns, N_P, as shown previously. Calculate B_M from peak current, I_P, number of primary turns, N_P, effective gapped inductance, A_{LG}, and effective core cross-sectional area, A_E. You can also calculate B_M from effective dc input voltage (V_{MIN}–V_{DS}), output voltage, V_O, output diode voltage, V_D, and duty cycle, D:

$$B_M = \frac{N_P \times I_P \times A_{LG}}{10 \times A_E} = N_S \times \frac{I_P \times A_{LG}}{10 \times A_E} \times \frac{V_{MIN} - V_{DS}}{V_O + V_D} \times \frac{D}{1-D}.$$

B_{AC} is the ac-flux density component. The equation gives peak ac-flux density (rather than p-p) to use with core loss curves, which the core vendor provides. Calculate B_{AC} from maximum flux density, B_M, and ripple-to-peak-current ratio, K_{RP}. You can also calculate B_{AC} from effective primary voltage, duty cycle, frequency, effective core cross-sectional area, and number of primary turns, N_S:

$$B_{AC} = \frac{B_M \times K_{RP}}{2} = \frac{(V_{MIN} - V_{DS}) \times D \times 10^8}{2 \times f_S \times A_E \times N_P}.$$

Gap length, L_G, is the air gap ground into the center leg of the transformer core. Grinding tolerances and A_{LG} accuracy place a minimum limit of 2 mils on L_G. Calculate L_G from the



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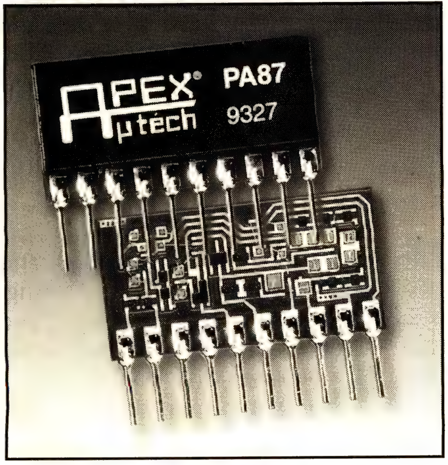

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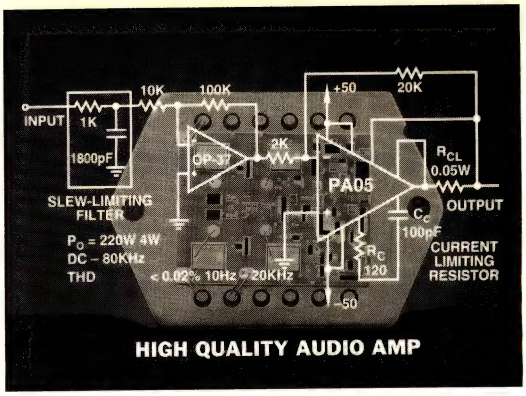

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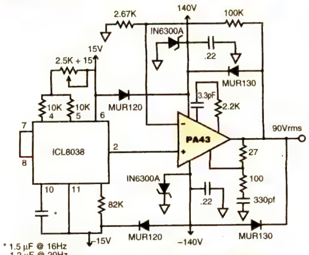

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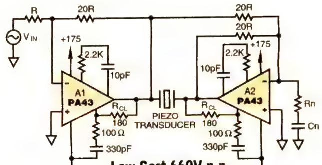

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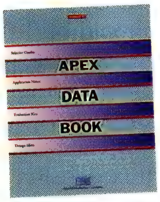

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Circle #115 in U.S. Circle #116 in Europe number of primary turns, N_P, core-effective cross-sectional-area, A_E, primary inductance, L_P (in microhenries), core effective path length, L_E, and relative permeability, μ_r:

$$L_G = \left(\frac{0.4\times\pi\times N_P^2 \times A_E}{L_P\times 100} - \frac{L_E}{u_r}\right)\times\frac{10^3}{2.54}.$$

Magnet wire for transformer winding usually has the cross-sectional area specified in circular mils. Circular mils per amp (CMA) is a convenient way to specify winding current capacity. CMA, which is the inverse of current density, is simply the ratio of cross-sectional area in circular mils to the rms value of primary current. Calculate CMA, which should range from 200 to 500, from wire diameter DIA (mils) and rms primary current, I_{RMS}.

$$CMA = \frac{1.27\times DIA^2 \times \frac{\pi}{4}}{I_{RMS}}$$

You've now completed all calculations necessary for the primary winding. Now you must calculate secondary rms current, secondary minimum and maximum conductor diameter, and number of bias winding turns. Derive secondary rms current, I_{SRMS}, from duty cycle, D, primary peak current, I_P, primary and secondary turns, N_P and N_S, and ripple-to-peak-current ratio, K_{RP} (same for primary and secondary):

$$I_{SRMS} = I_P\times\frac{N_P}{N_S}\times\sqrt{(1-D)\times\left(\frac{K_{RP}^2}{3} - K_{RP} + 1\right)}.$$

Determine minimum secondary conductor diameter, DIA_{SEC} (in mils), based on previously calculated current capacity, CMA, and secondary rms current.

$$DIA_{SEC} = \sqrt{\frac{4\times CMA\times I_{SRMS}}{1.27\times\pi}}$$

Calculate the maximum wire outside diameter, OD_{SEC} (in mils), for a single layer based on number of secondary turns and bobbin width:

$$OD_{SEC} = 1000\times\frac{B_W - (2\times M)}{N_S}.$$

For magnet-wire secondaries, the minimum conductor diameter, DIA_{SEC}, should be less than the maximum outside diameter, OD_{SEC}. Use larger magnet wire with a diameter equal to OD_{SEC}. For insulated wire secondaries, specify a conductor diameter width equal to or greater than DIA_{SEC} and an insulated outside diameter less than or equal to OD_{SEC}. Parallel combinations of wire with half the diameter may be easier to wind and terminate. Finally, calculate the number of bias-winding turns, N_B, from the output voltage, V_O, output diode voltage, V_D, primary and secondary number of turns, N_P and N_S, respectively, target bias voltage, V_B, and bias diode voltage, V_{BD}:

$$N_B = \frac{V_B + V_{BD}}{V_O + V_D}\times N_S.$$

To reduce the number of wire gauges necessary in production, the bias winding is usually wound with the same wire diameter as the primary. You can also use this equation to specify other windings for multiple-output-voltage applications.

Calculate voltage-stress parameters

Reflected output voltage, V_{OR}, is the voltage appearing across the primary when the transistor is off and current flows through the output diode. V_{OR} depends directly on output voltage, V_O, diode voltage, V_D, and transformer primary and secondary number of turns, N_P and N_S, respectively. Calculate V_{OR} from duty cycle, D, minimum dc input voltage, V_{MIN}, and MOSFET on-state voltage, V_{DS}.

$$V_{OR} = (V_O + V_D)\times\frac{N_P}{N_S} = (V_{MIN} - V_{DS})\times\frac{D}{1-D}$$

Maximum drain voltage (excluding leakage-inductance-induced spikes) is simply the sum of maximum dc input voltage, V_{MAX}, and reflected output voltage, V_{OR}:

$$V_{DRAIN} = V_{MAX} + V_{OR}.$$

Determine maximum peak inverse voltage, V_{PIV}, for the output rectifier by transformer primary and secondary numbers of turns, N_P and N_S, respectively, maximum dc input voltage, V_{DC}, and output voltage, V_O. Calculate V_{PIV} from minimum dc input voltage, V_{MIN}, MOSFET on-state voltage, V_{DS}, output diode voltage, V_D, and duty cycle, D:

$$V_{PIV} = V_O + \left(V_{MAX}\times\frac{N_S}{N_P}\right) = V_O + \left(V_{MAX}\times\frac{V_O + V_D}{V_{MIN} - V_{DS}}\times\frac{1-D}{D}\right).$$

Before beginning iteration, check the V_{DRAIN} voltage and compare with the TOPSwitch-breakdown-voltage rating. TOPS100 series parts should have at least 50V of margin, and TOPS200 series parts should have at least 100V of margin for clamping leading-edge spike voltages that leakage inductance causes. Reduce duty cycle, D, minimum ac input voltage, V_{ACMIN}, or input capacitor, C_{IN}, to reduce stress voltage, V_{DRAIN}.

Use iteration to reach a final and acceptable solution for the flyback-transformer design. Iterate peak current, I_P, until the ripple-to-peak ratio, K_{RP}, is within indicated limits. K_{RP} should be 1.0 for discontinuous operation and small transformer size, 0.33 for heavy continuous design and best efficiency, or approximately 0.66 for a good trade-off between the two. K_{RP} will decrease as peak current, I_P, is reduced.

Iterate number of secondary turns, N_S, until maximum flux density, B_M, falls between indicated limits. Check that the gap length, L_G, is higher than indicated minimum value. B_M will decrease and L_G will increase as the number of secondary turns, N_S, increases.

Examine primary current capacity in CMA. If CMA is below the specified lower limit of 200, consider increasing number of primary layers from one to two or use the next larger core and perform new iteration. If CMA is greater than

(continued on pg 113)

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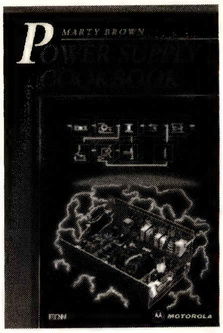

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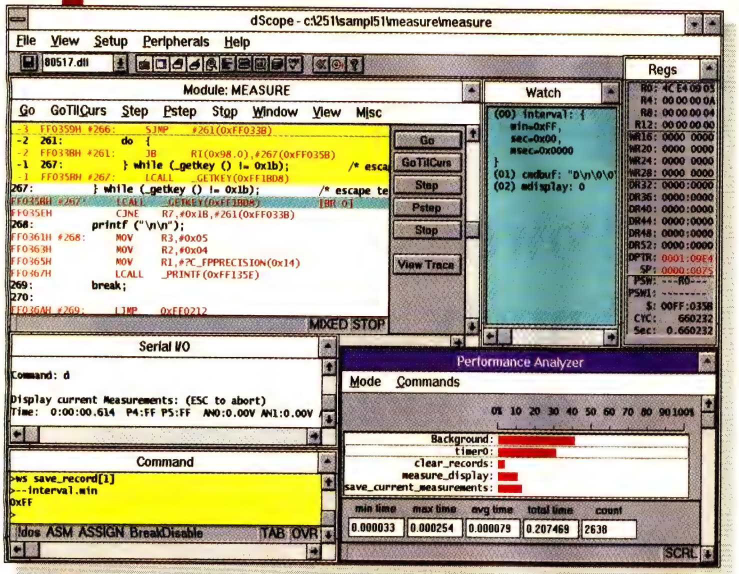
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80517.dll
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Go
GoTilCurs
Step
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Stop
View Trace
MIXED STOP
Watch
Regs
Serial I/O
Performance Analyzer
Mode Commands
Command
!dos ASM ASSIGN BreakDisable TAB OVR
SCRL

```
 -3  FF0359H #266:     SJMP    #261(0xFF033B)
 -2  261:            do  {
 -2  FF033BH #261:     JB      RI(0x98.0),#267(0xFF035B)
 -1  267:              } while (_getkey () != 0x1b);          /* esca
 -1  FF035BH #267:     LCALL   _GETKEY(0xFF1BD8)
267:             } while (_getkey () != 0x1b);          /* escape te
FF035BH #267:    LCALL   _GETKEY(0xFF1BD8)              [BR 0]
FF035EH          CJNE    R7,#0x1B,#261(0xFF033B)
268:             printf ("\n\n");
FF0361H #268:    MOV     R3,#0x05
FF0363H          MOV     R2,#0x04
FF0365H          MOV     R1,#?C_FPPRECISION(0x14)
FF0367H          LCALL   _PRINTF(0xFF135E)
269:             break;
270:
FF036AH #269:    LJMP    0xFF0212
```

```
(00) interval: {
    min=0xFF,
    sec=0x00,
    msec=0x0000
}
(01) cmdbuf: "D\n\0\0"
(02) mdisplay: 0
```

```
  R0: 4C E4 09 05
  R4: 00 00 00 0A
  R8: 00 00 00 04
 R12: 00 00 00 00
WR16: 0000  0000
WR20: 0000  0000
WR24: 0000  0000
WR28: 0000  0000
DR32: 0000:0000
DR36: 0000:0000
DR40: 0000:0000
DR44: 0000:0000
DR48: 0000:0000
DR52: 0000:0000
DPTR: 0001:09E4
  SP: 0000:0075
 PSW: ---R0---
PSW1: --------
   $: 00FF:0358
 CYC:     660232
 Sec:   0.660232
```

```
Command: d

Display current Measurements: (ESC to abort)
Time:  0:00:00.614  P4:FF P5:FF   AN0:0.00V AN1:0.00V
```

```
>ws save_record[1]
>--interval.min
0xFF
>
```

min time	max time	avg time	total time	count
0.000033	0.000254	0.000079	0.207469	2638

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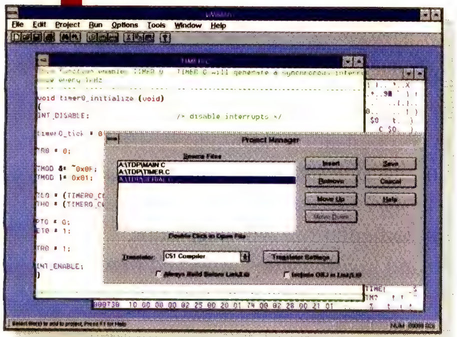

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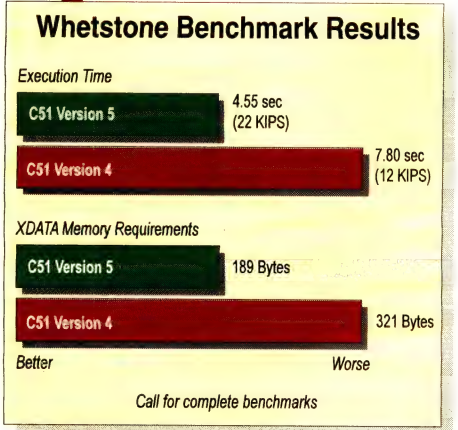

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Reference

1. McLyman, C, *Transformer and Inductor Design Handbook*, Marcel Dekker Inc, 1978.

Author's biography

Brooks R Leman is a senior applications engineer at Power Integrations Inc (Mountain View, CA), where he has worked for six years. He develops low-cost flyback and PFC circuits using highly integrated power-supply devices. Leman has a BSEE and an MSEE from Santa Clara University (Santa Clara, CA) and is a member of the Tau Beta Pi professional society. His hobbies include soccer and skiing.

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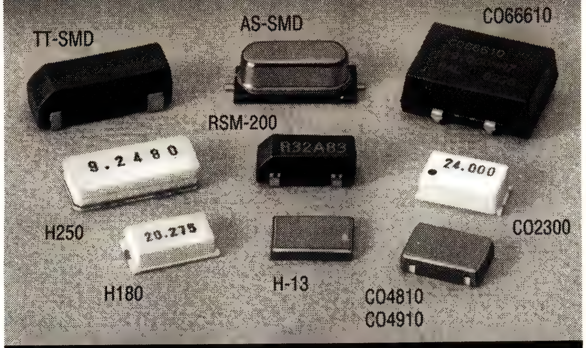

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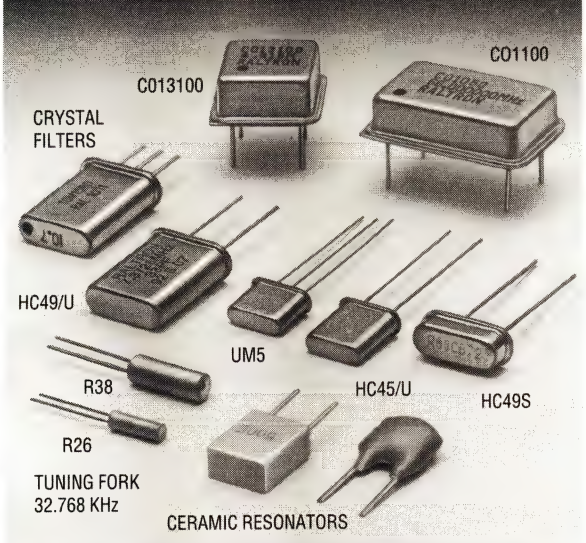

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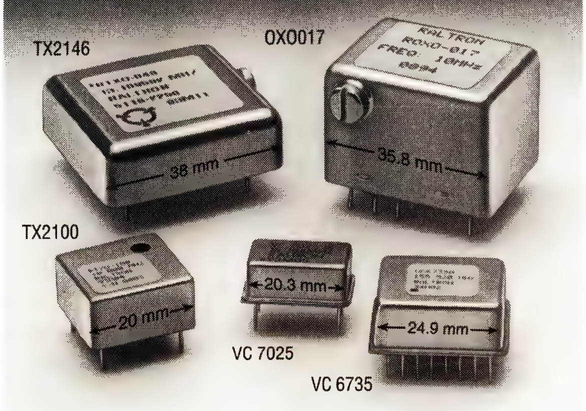

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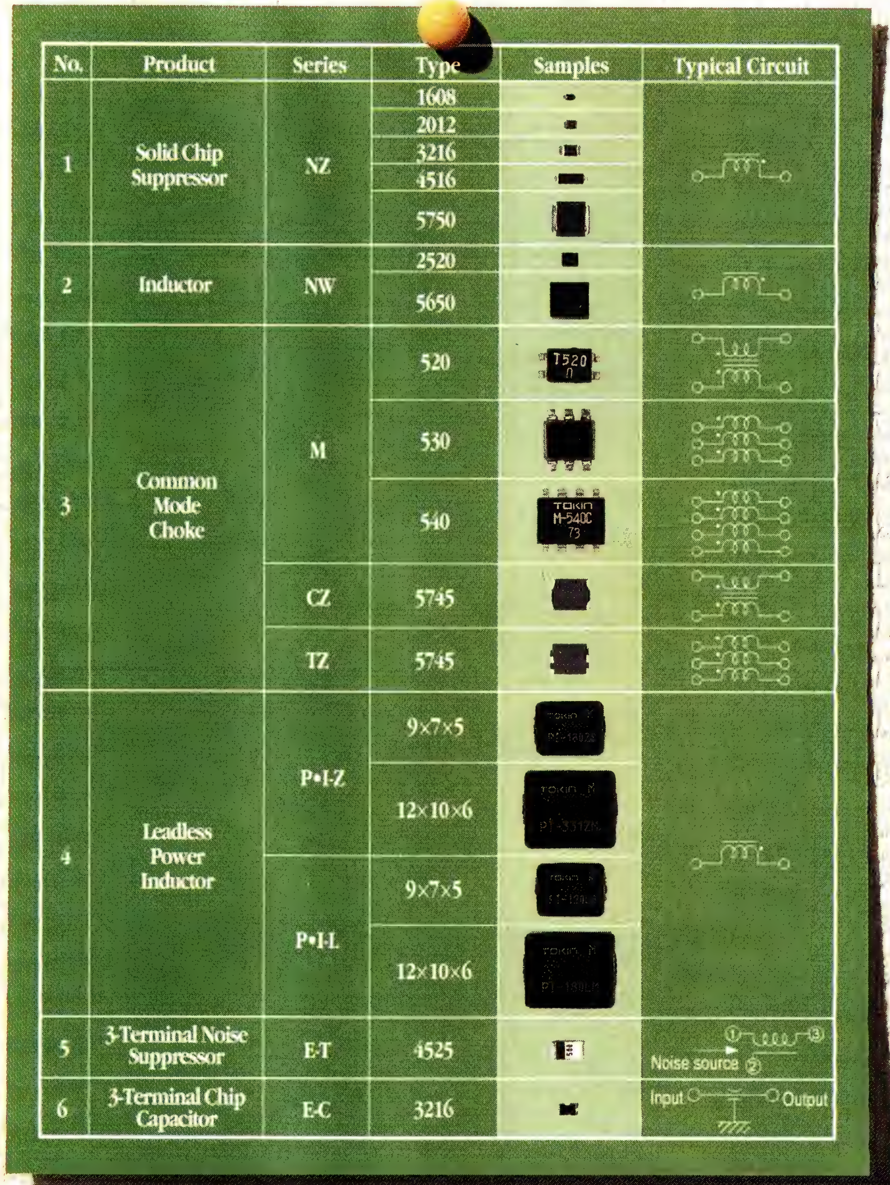

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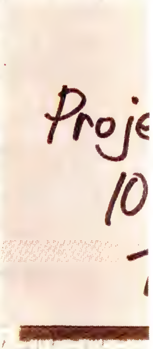

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CIRCLE NO. 217

DMA module enhances μC CPU performance

KEVIN ANDERSON, MOTOROLA INC

Matching a μC's CPU performance to a particular application can be a tricky task. However, to enhance μC performance, a DMA module peripheral can offload many data-transfer tasks from the CPU—and help you defray overall system cost.

When selecting a single-chip μC for an embedded application, consider CPU performance. If the application requires a large number of 16-bit multiplies in a 1-msec timing loop, a CPU that can handle half that number is obviously inadequate. On the other hand, choosing a high-performance CPU to perform simple routines such as scanning a keypad and sending encoded output may result in an end product that is too costly.

Another key issue in selecting a μC involves the capabilities of the peripheral subset on the μC. A well-designed peripheral subset can stretch the performance of a low-cost CPU, which ultimately can drive down system costs.

One example of a peripheral that increases CPU performance is an on-chip DMA module. Traditionally, designers have used DMA to move large blocks of data efficiently within a system. Current μC architectures, such as Motorola's HC08 CPU, have extensions that allow for additional on-chip processing modules. In such cases, you can use a DMA module to perform peripheral service routines. Using this capability can significantly decrease peripheral service latency and increase effective CPU efficiency. The bulk of this article describes the DMA implementation for a single-chip μC in an embedded application; it also includes programming examples that demonstrate how DMA can provide significant and improved system performance.

DMA serves as a means of transferring data between memory and buffers without CPU intervention. In a single-chip μC, large data-block moves are not common, because these devices usually operate independently in a system and are not connected through a bus structure to other CPUs and memory systems. In addition, latency and overhead are associated with entering and exiting an interrupt service routine (see **box**, "Consider both latency and overhead"). However, once initialized, DMA can service numerous transmit requests without further code execution, and it only interrupts the CPU after the entire message is sent. Transferring each byte takes only two cycles, contrasting with the dozens of cycles needed for CPU service.

Old burglars never die

The DMA operates by stealing cycles from the CPU (see **box**, "Architectural features aid DMA performance"). For

ARCHITECTURAL FEATURES AID DMA PERFORMANCE

Three architectural features of HC08-family μCs contribute to the chips' ability to perform DMA functions. First, the peripherals are memory-mapped, which means the CPU's address space can access control and status registers. Thus, any instruction that can access memory can also access a peripheral so the access doesn't require special peripheral service routines. Similarly, the DMA module can also access the peripheral registers as just another space in the memory map.

Second, the HC08 CPU allows on-chip co-processor modules to take control of the system address and data buses at a bus-cycle boundary. Motorola designed the co-processors to retain bus control until they've finished their business or can allocate a certain maximum percentage of the bus bandwidth to the co-processor. The latter method is known as "cycle stealing" and allows for overlap between the CPU and the co-processor.

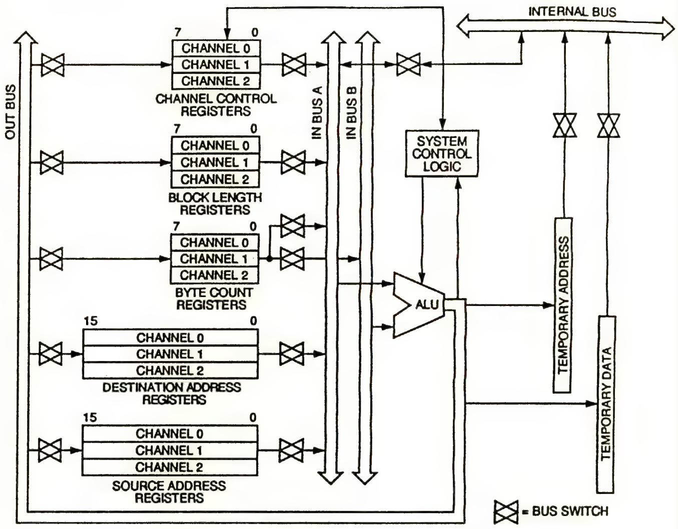
Finally, Motorola designed the peripheral modules with hooks into the DMA module. You can initialize each module having DMA service, so that an interrupt-service request is directed to the DMA module rather than to a CPU interrupt. You can also set up a DMA channel to handle the interrupt request from the peripheral. Once initialized, the DMA module can service the peripheral without CPU code execution and with only two-cycle latency vs the minimum of nine cycles for CPU service.

each group of bytes transferred, DMA takes over the data and address buses for two cycles. Once the transfer completes, the CPU immediately regains control of the bus and continues operation. In low-data-rate situations, such as 9600-baud serial transfers, the number of cycles taken from the CPU is a very small percentage of the total cycles. If the application requires quick transfer of large amounts of data, such as moving a table of saved values from EEPROM to RAM, DMA transfer can take over the entire bus bandwidth. Large data transfers effectively halt the CPU; however, the overall efficiency remains high because the DMA transfer occurs in fewer cycles than a CPU transfer.

Fig 1 shows the DMA module in the HC08. Each DMA channel has its own set of programmable registers; the CPU can read or write to all of the registers. You program the base address of the data source and destination into the source and destination registers. These registers are 16 bits wide and can point to any place in the μC's memory space. The block-length register sets the total number of bytes to transfer.

The DMA module can transfer as many as 256 bytes in a block. The DMA module clears the byte-count register before a block transfer begins. After initialization, the byte-count register increments for each byte transferred. The DMA's ALU uses this value in calculating the source and destination address during a block transfer. The CPU may read this register at any time to determine how many bytes out of the total have been sent.

FIGURE 1



A block diagram of the DMA module in the HC08 μC shows the internal registers and buses used to perform DMA operations.

Control registers assign service

Each channel also has a channel-control register, which lets the μC assign service to any specific peripheral. The channel-control register also selects whether the DMA module will send one or two bytes in a single transfer. Two byte transfers occur consecutively and take four cycles to complete.

In addition, the channel-control registers control source and destination address generation. The channel source and destination addresses may be set to increment, decrement, or remain static as each byte transfers. Flexible address-generation control is key to the DMA module's ability to service peripheral modules. For example, if you're using DMA to move a data table from ROM to RAM on power-up, you set both source and destination registers to increment. In a different scenario, you might use DMA to service an A/D converter connected to the serial peripheral interface (SPI). Here, the source points to the SPI data register and remains static while the destination address increments and stores successive bytes in a receive buffer. Alternatively, the destination address could remain static, in which case the CPU always has access to the latest A/D-converter value.

TABLE 1— DMA-VS-CPU BLOCK-MOVE PERFORMANCE

Block size	CPU clocks	DMA clocks	Relative performance
8	90	46	2.0
16	178	62	2.9
32	354	94	3.8
64	706	158	4.5
128	1410	286	4.9
256	2818	542	5.2

The DMA module has a set of system status and control registers that control other module options. Each channel can be individually enabled, set to interrupt the CPU at the end of a transfer block and to loop back to the beginning of a transfer once a block has completed. This last capability allows you to create a process that can run forever without CPU intervention. The bus bandwidth available for DMA operations is also programmable. You can set the bandwidth to allow 25, 50, 67, or 100% of the bus cycles available for DMA operation.

A couple of examples would help to illustrate the DMA module's performance-enhancement capability. A common software routine found in embedded-control-initialization code is the block move. This routine can clear a section of memory or copy a table from program ROM to RAM; another use for it is when system variables store to RAM, where they are modified without using an EEPROM erase or programming cycle. At power- down, another routine saves the modified values back to EEPROM so that new values are available at the next power-up.

CPU transfers block data

Example 1 shows an in-line software block move similar to that found *in initialization* pseudo-code. This routine transfers data between any two blocks within a 16-bit address space. To express the total number of CPU cycles consumed in transferring N bytes, use

$$T_{CPU}=13+11(N-1).$$

Example 1—CPU-block-move pseudo-code

```
while source_address > source_bottom_address -1
     move from source_address to destination_address
     decrement source_address
     decrement destination_address
```

To examine the impact of using DMA, note the pseudo-code in **Example 2**, which shows the code for the case above.

Example 2—DMA-block-move pseudo-code

```
move source_start_addr to source_pointer
move destination_start _addr to destination_pointer
move transfer_setup to control_registers
enable transfer
```

You initialize the DMA channel with the number of bytes to be transferred as well as the source and destination pointers. The channel is also set to use 100% of CPU bandwidth. You initiate the transfer by writing to a DMA control register, which allows software to start a DMA transfer. To determine the total number of CPU cycles used to transfer N bytes in this manner, use

$$T_{DMA}=init+2N=30+2N.$$

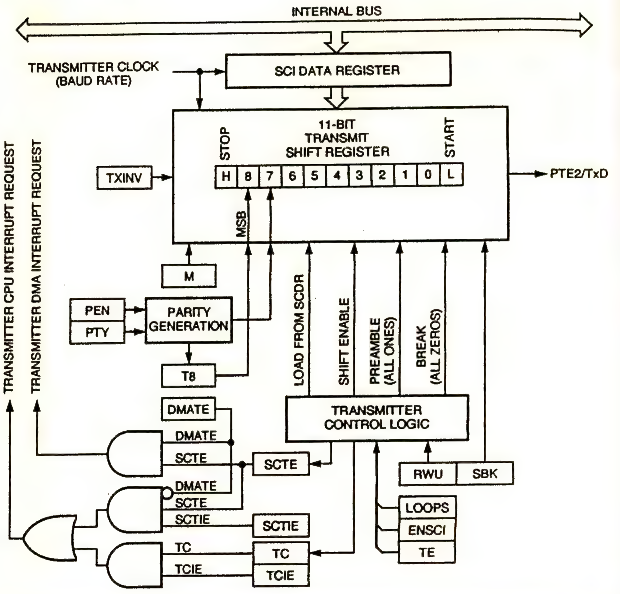
Table 1 lists the number of cycles required for various transfer sizes and relative performance improvement when opting for DMA over CPU transfer.

Using the data from the two equations above, it is evident that, for transfers of more than 3 bytes, the DMA-transfer method is quicker. However, another factor to consider is the amount of code space each routine uses. The CPU-transfer code takes 10 bytes, whereas the DMA initialization code takes 22. Therefore, you may need to choose between execution speed and program size if you expect the program memory to fill completely.

Use DMA for large serial transfers

Example 3 demonstrates use of the DMA module with an onboard peripheral, the serial communications interface (SCI). **Fig 2** shows a simplified block diagram of the SCI transmitter logic. Once the SCI is initialized and enabled, transmission begins when you write a character to the SCI data register. The SCI immediately transfers this character into the transmit-shift register and, under control of the transmit control logic, shifts the bits out to the transmit pin at the programmed baud rate. When the character moves from the SCI bus to the transmit-shift register, the SCI sets the transmit-data-register-empty flag and sends an interrupt request to the CPU.

FIGURE 2



This simplified block diagram of the logic in an SCI transmitter demonstrates the use of DMA with an onboard peripheral.

Example 3—SCI transmit using CPU-interrupt pseudo-code

```
* Initialize the SCI

initialize serial_transfer_registers
enable serial_transmitter
enable CPU_interrupts



* SCI Transmit Interrupt Service Routine

get next_byte_address
if next_byte_address<last_byte_address
then
     clear flags
     move byte to transmit_register
     increment next_byte_address
     save next_byte_address
else
     disable serial_transmitter
     disable CPU_interrupts
```

Example 3 shows the pseudo-code required to initialize the SCI and transmit a message using CPU interrupts. This example assumes that another routine has placed a message in the transmit-buffer space, which begins at the pointer TXADDR, and has initialized the TXEND pointer to the next byte following the end of the message. The code begins with the steps needed to initialize the SCI, including the transfer format and the baud rate, and to enable the SCI and CPU interrupts.

The transmit interrupt-service routine (ISR) checks the TXADDR pointer and compares it with the TXEND pointer to determine if the end of the buffer has been reached. If not, the CPU moves the byte specified by the TXADDR pointer to the SCI transmitter data register (SCD), increments the pointer by one, and clears the flag before exiting the routine. If the two pointers are equal, the complete message has been transferred and the routine ends by disabling the transmitter.

Now, analyze this routine to find the number of CPU cycles required to transmit a message of arbitrary length. Initializing the SCI takes 14 cycles. For every character transmitted, the CPU executes 29 cycles, plus a minimum of nine cycles to enter the ISR. While the CPU shifts the last character out, the CPU generates one final ISR, which takes the branch to disable the transmitter (TCEND). The process takes 26 cycles, plus nine overhead cycles. For a message of length N, the total is

$$T_{cycles}IRQ=14+N(29+9)+(26+9)=38N+49.$$

The actual number will be somewhat larger because the CPU can take interrupts only on instruction boundaries. Therefore, it is likely that one or more additional cycles of latency will occur for each interrupt-service entry.

CPU-vs-DMA serial-data transmission

You can compare these results with the number of cycles needed to make the same transfer using the DMA module to service the transmit interrupt. **Example 4** shows the pseudocode required. The CPU must initialize the SCI except that the DMA handles the transmit-data-register-empty (TDRE) interrupts. The DMA setup involves initializing the DMA source and destination address (TXADDR and SCD, respectively), setting the block length (number of bytes to be transferred), setting the transfer type (increment the source address and hold the destination address static), and assigning the channel to service the SCI TX interrupt. The DMA module will also enable a CPU interrupt once the last DMA transfer has taken place. The process takes 27 cycles.

EXAMPLE 4—SCI TRANSMIT USING DMA PSEUDO-CODE

```
* Initialize the SCI DMA transfer

initialize serial_transfer_registers
move source_start_addr to source_pointer
move destination_start _addr to destination_pointer
move transfer_setup to control_registers
enable transfer
enable CPU_interrupts



* DMA interrupt service routine

disable transmitter
disable CPU_interrupts
clear flags
```

Once the DMA module enables the SCI transmitter, each byte takes two bus cycles. After the last DMA transfer has completed, the DMA module issues an interrupt to the CPU. The ISR checks to see if this channel made the interrupt request. If so, the CPU disables the transmitter and clears the flag. The number of clock cycles equals 24, plus nine to enter the ISR. To derive the total number of cycles to transfer N bytes, use

$$T_{cycles}DMA=45+N(2)+(24+9)=78+2N.$$

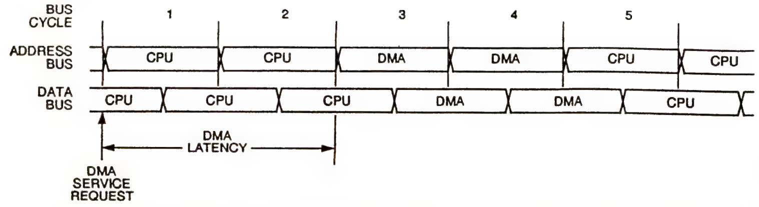
CONSIDER BOTH LATENCY AND OVERHEAD

The HC08 DMA-peripheral-service latency can be as low as two bus cycles (**Fig A**). This condition occurs when you set the DMA module for 100% bandwidth or when the CPU has received the minimum number of bus cycles since the last DMA transfer. Normal CPU-interrupt-service latency is nine bus cycles. Thus, the best case latency improvement using the DMA module is 4.5 times the interrupt-service-routine (ISR) latency. Latency can be an important parameter if fast peripheral service is imperative.

However, latency is only one factor to consider; the other is overhead, *which* is defined as the number of CPU bus cycles required to enter and exit the ISR. The HC08 CPU takes nine bus cycles to enter an ISR and seven cycles to exit—for a total of 16 cycles.

Overhead is in addition to the number of cycles the CPU uses to actually execute the service routine. Service of the ISR by the DMA module does not incur overhead, because the CPU has control over the bus and can do useful work during the latency period before the DMA channel actually receives the bus.

FIGURE A



The latency required to service a DMA transfer can be as low as two bus cycles.

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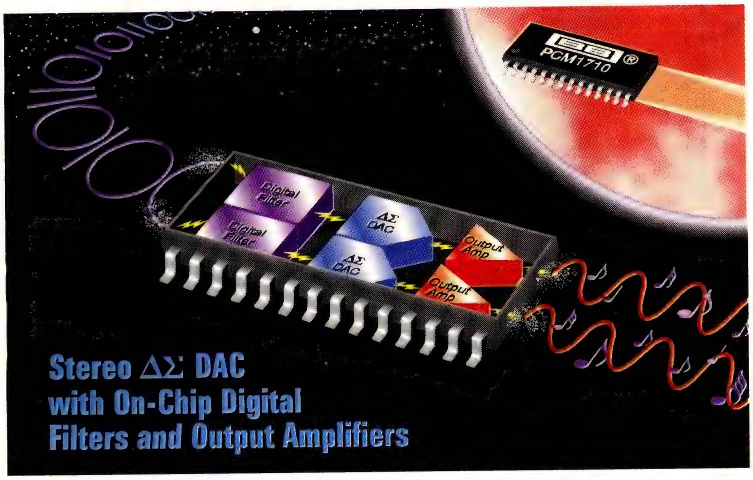
CIRCLE NO. 26

New



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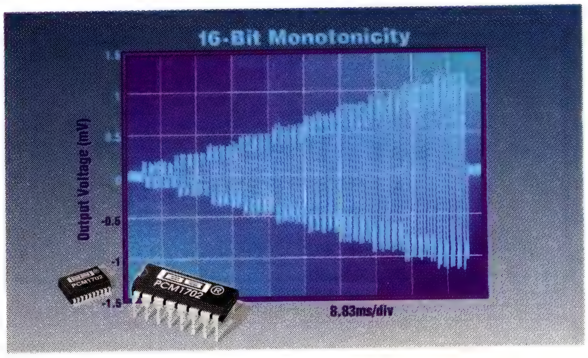

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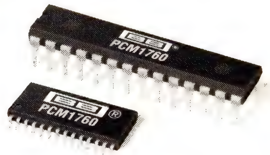

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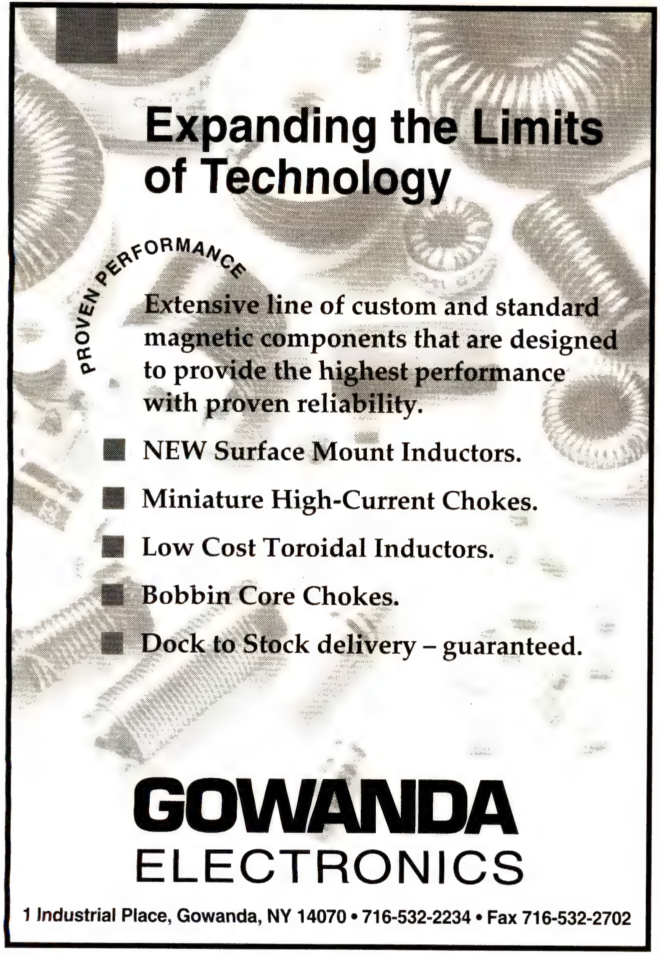
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TABLE 2—DMA-VS-CPU SCI-TRANSMIT PERFORMANCE BLOCK

Block size	CPU clocks	DMA clocks	Relative performance
1	87	80	1.1
2	125	82	1.5
3	163	84	1.9
4	201	86	2.3
5	239	88	2.7
6	277	90	3.1
7	315	92	3.4
8	353	94	3.8
9	391	96	4.1
10	429	98	4.4
15	619	108	5.7
20	809	118	6.9

Table 2 shows the number of cycles needed by each method for several transfer sizes. The number of cycles to transfer even 1 byte is fewer using the DMA method. The number of bytes of code is larger in the DMA case (this time by 14 bytes), but, in most instances, the additional throughput improvement is far greater than the number of additional bytes of code.

The examples listed above show just a few possible uses of DMA within the μC architecture. In conjunction with other peripheral modules, you can devise many other applications. For example, in concert with a timer, you can implement a fast, flexible, variable-duty-cycle PWM requiring only one timer channel and no CPU intervention. EDN

Author's biography

Kevin Anderson is a field applications engineer for Motorola's Semiconductor Products Sector. Anderson develops applications and performs engineering for automotive electronics. He has helped to develop several versions of 68HC05, 68HC08, 68HC11, and 68300 μCs. Anderson earned a BSEE from South Dakota State University (Brookings, SD) and is a member of the IEEE and Society of Automotive Engineers. In his spare time, he enjoys music, boating, and the outdoors.

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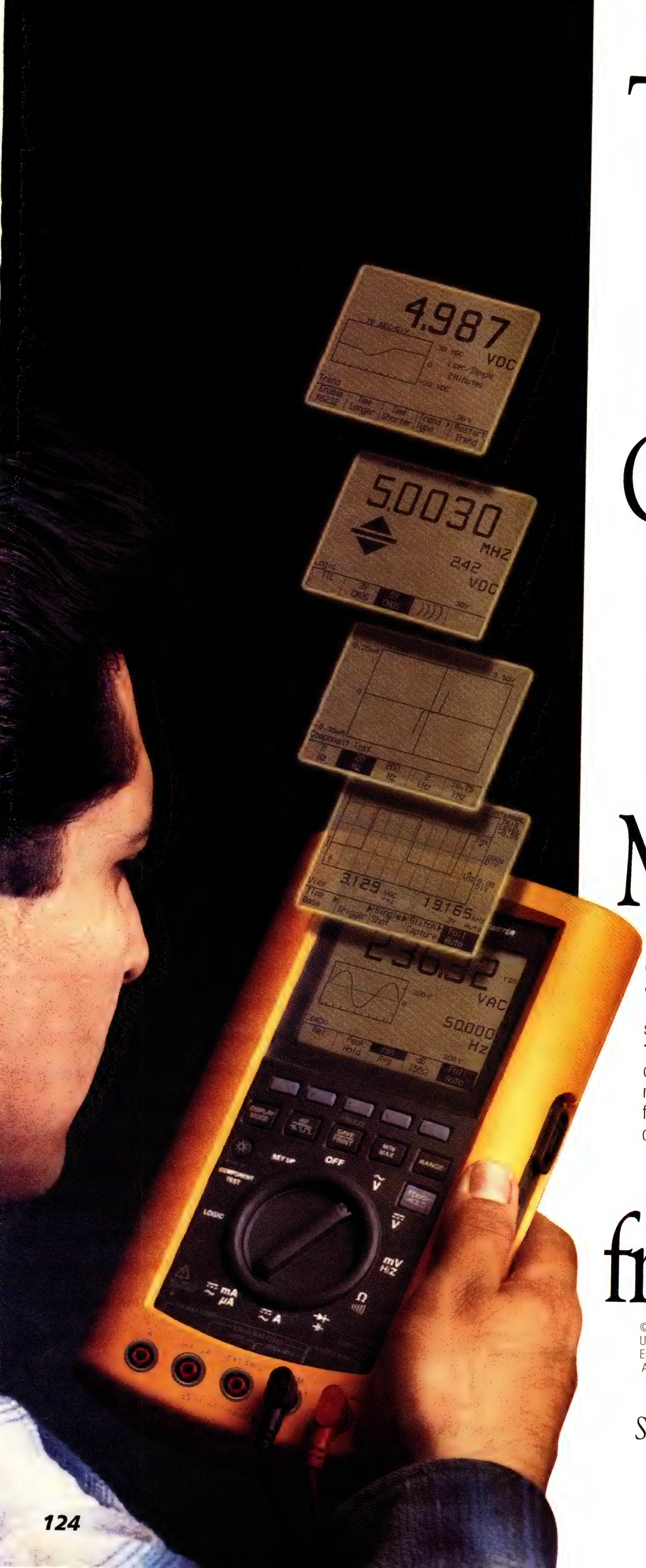

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STEP: a new standard for EDA tools

LARS CELANDER, INSTITUTET FÖR VERKSTADSTEKNISK FORSKNING

Surveys show that useful standards—not more bells and whistles—are what users need and want. Until now, EDIF and CFI, which offer limited usefulness, were the only standards available to meet those needs. Now, a new standard, STEP, has emerged and may well turn out to be exactly what users have been awaiting.

Solid, effective, reliable, and well-supported standards are rare. Although users need and want such standards, electronic-design-automation (EDA) tool vendors have been slow to support them. The situation is particularly unfortunate in the area of populated pc boards. A number of standards are in use, but they provide only partial—and ineffective—results, including Gerber, the Electronic Design Interchange Format (EDIF), and the CAD Framework Initiative (CFI). To make up for the lack of standards, the EDA industry has borrowed geometry-oriented standards from mechanical engineering, such as IGES and DXF, for drawings, board outlines, and the like. However, these standards, too, meet only some of the users' requirements.

Now, the Standard for the Exchange of Product Model Data (STEP) is emerging as a powerful, professional standard and a model for similar standards in other areas. Developers within the ISO spent considerable resources developing STEP as a standard for product descriptions, and the end result is impressive (see **box**, "Who develops STEP?"). STEP encompasses a wide range of products, and it covers the products' entire life cycle.

The first of the standards preceding STEP was Gerber, which takes its name from its developer, a photo-plotter manufacturer. Gerber developed the standard as an internal file format describing pc-board layout. Gerber lists commands for a photo plotter and a drilling machine and includes pure graphics with no "intelligence" whatsoever. Gerber has been around a long time, and it works well. More important, nearly every vendor supports Gerber. Despite its advantages, however, Gerber does not integrate well with the other dominant standards.

The next standard to emerge was EDIF, a file format launched in the mid-80s that enabled users to exchange netlists. Over the years, developers have added more and more "speed stripes," but EDIF still effectively handles only netlists. How well EDIF works depends largely on the skill and experience of its users. EDIF-PCB, which extends EDIF from netlists to layouts, is in the works.

The latest major standards effort, CFI, emerged from a group of tool vendors who wanted to achieve better interoperability among their tools. CFI lets users of Unix workstations perform exchanges in real time of netlists among tools from different vendors. Thus, CFI not only defines the data to be exchanged and the mechanism with which to do it, but also includes specifications for communication, windowing, and process interaction. However, like EDIF, CFI effectively supports only netlists. It also lacks facilities for archiving, for exchanging data off-line, and for exchanging data between tools in distributed and heterogeneous environments. These requirements are critical for users who want to replace one vendor's tool with that of another vendor.

CFI's developers are planning a major rewrite to combat these deficiencies. The rewrite will probably add a file format, enable communication among mixed platforms, and remove some of the communication and windowing specifications, leaving those areas to the various operating systems. Like EDIF, CFI will also eventually expand the data it handles beyond simple netlists.

Standards soup

All these standards make for a messy situation. With the exception of Gerber, none of the standards works well; integration among them is nonexistent; and attempting to use them as a group is hopeless. Mechanical engineering has long grappled with the same problems, albeit on another scale and with a different set of market dynamics. However, the mechanical-engineering industry has matured past the IGES and DXF stage and is now moving on to STEP.

STEP standardizes on two levels. First, it specifies the "information model," that is, the concepts and the terminology an application uses. The underlying information model ensures that the receiver can correctly understand the meaning of the information. Second, STEP specifies the actual exchange mechanisms to transfer the information.

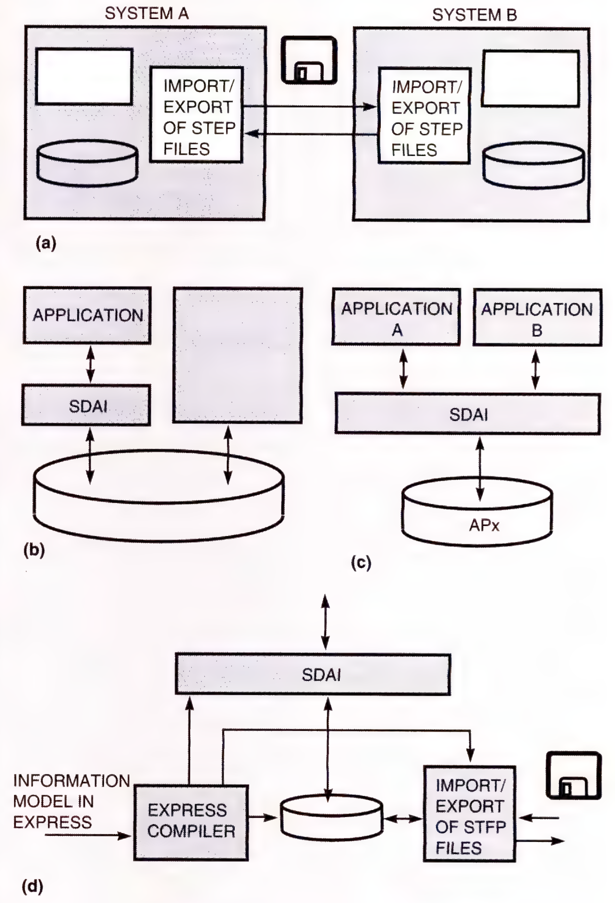
STEP's modular architecture allows application areas to have different information models. Application protocols (APs) define these models, which are the most outwardly visible parts of STEP. The information models are all written in Express, an information-modeling language that STEP defines. Although splitting STEP into APs makes the standard more flexible and manageable, the division raises the question of interoperability among APs. To handle this problem, STEP uses an infrastructure for integrating data from different application areas.

STEP includes two exchange mechanisms, a file format and the Standard Data Access Interface (SDAI), an application-programming interface for on-line communication. The file format works in a way similar to the file formats of EDIF and IGES. SDAI is an on-line communication interface similar to CFI. The mechanisms exchange data that are independent of the mechanisms themselves. Instead, the mechanism making a reference to an Express model defines the data.

Ask to see the certificate

STEP lets independent labs test conformance against the standards. These labs can issue certificates of conformance to products that claim to support STEP. For a buyer of a system requiring STEP compliance, life is easy: Ask your vendor to show that certificate. This document gives STEP the teeth to ensure that things work reliably in practice.

FIGURE 1


SYSTEM A
SYSTEM B
IMPORT/ EXPORT OF STEP FILES
IMPORT/ EXPORT OF STEP FILES
(a)
APPLICATION
SDAI
(b)
APPLICATION A
APPLICATION B
SDAI
APx
(c)
SDAI
INFORMATION MODEL IN EXPRESS
EXPRESS COMPILER
IMPORT/ EXPORT OF STFP FILES
(d)

You can use STEP to exchange files (a), in portable applications (b), as a standard database (c), or as a tool for application development (d).

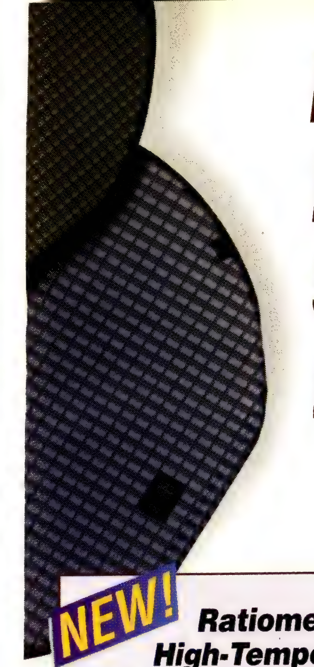
WHO DEVELOPS STEP?

The ISO Technical Committee 184, Subcommittee 4 (TC184/SC4) developed the Standard for the Exchange of Product Model Data (STEP). Industry participants and independent organizations perform the ISO work, which is voluntary, self-financed, and open to anybody. User requirements—not vendors—drive the work, although several CAD vendors are actively working on STEP.

The SC4 votes on all major decisions within STEP, such as elevating a draft standard to an International Standard. The member nations in SC4, roughly in order of the size of their delegations, are the United States, the United Kingdom, Germany, France, Switzerland, Sweden, the Netherlands, Norway, Japan, Italy, Canada, Australia, Belgium, Hungary, Brazil, Romania, and Russia.

Since, 1987, The Institutet för Verkstadsteknisk Forskning (IVF) (the Swedish Institute of Production Engineering Research) has been participating in the work to develop STEP. IVF is also involved in various activities to educate the Swedish industry about the possibilities in STEP and how to most effectively employ STEP.

For more information about STEP or STEP-related activities, contact Lars Celander at +44 (31) 706 6116 or on Internet at lc@ivf.se.



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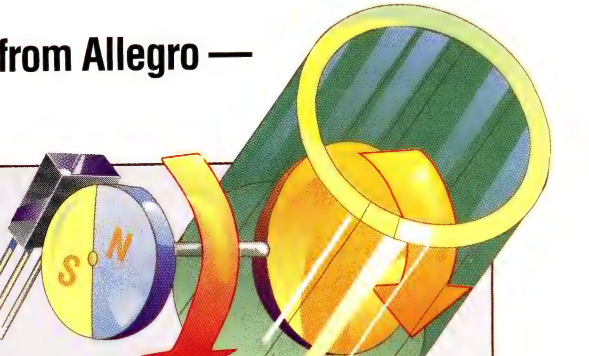

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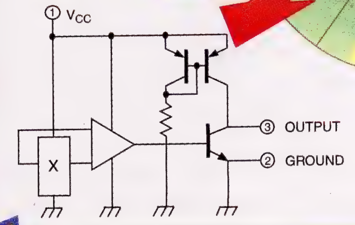

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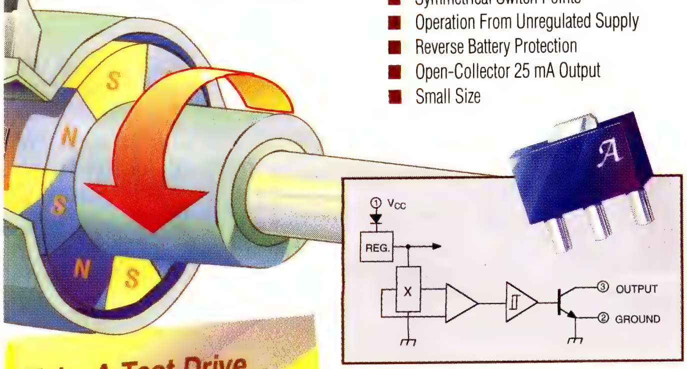

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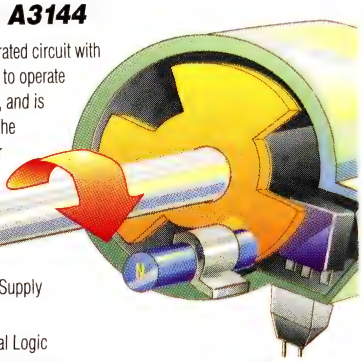

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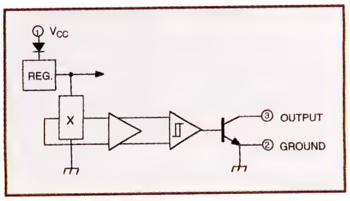

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Users have given STEP strong backing, and vendors view it as critical to the ability to compete in the market. Given this clear and well-financed backing, CAD system vendors are all supporting STEP. In addition, the mechanical-engineering, electrical-engineering, process, and architecture/engineering/construction industries will all employ STEP. The geographical-information-systems industry is also creating standards with an architecture similar to that of STEP and may use Express as the architecture's modeling language.

You can use STEP to exchange files, in portable applications, as a standard database, or as a tool for application development. In **Fig 1a**, the STEP file format exchanges files, and a user must specify which AP STEP is using. In **Fig 1b**, STEP uses SDAI as the standardized programming interface to the system database. An application written using SDAI and an AP can then move freely between a system having an SDAI for that AP. In **Fig 1c**, the content of an AP specifies the content of a database. All applications written using SDAI and that AP can then concurrently access that database. These applications serve as "editors" to an AP-defined database and are, therefore, fully interchangeable. In **Fig 1d**, the various tools within STEP act as an environment for application development with or without an AP. The advantages include possible use of STEP information models and the availability of standardized tools from several vendors.

A series of APs within STEP concerns printed-circuit assemblies. The first in this series is AP 210, "Printed Circuit Assembly Design and Manufacture." This AP supports netlist, component list, board layout, component placement, and administrative data. The AP does not support component data, except for geometry. AP 210's primary goal is to define the information that the design department passes on to manufacturing. AP 210 also works as a shared database for concurrent engineering. The information that describes the printed-circuit assembly is complete, is free of redundancy, includes precisely defined semantics, and comes in a vendor-independent form. From the ground up, AP 210 incorporates both electrical and mechanical characteristics—a critical requirement because many real-life problems result from a mix of these characteristics. AP 210 is then the ideal platform for realistic analog and digital simulation, EMI/electromagnetic-compatibility analysis, thermal analysis, verification of manufacturability, and archiving. The AP 210's vendor-independent database lets users mix any AP 210-compatible tools.

What now?

STEP is also affecting its standards' predecessors. For example, EDIF and CFI developers are rewriting both standards using Express. (VHDL also now uses Express.) However, even after their upgrades, EDIF and CFI remain merely subsets of AP 210.

Thus, we have a situation in which a technically superior standard (STEP) must attempt to overcome the current standards (CFI and EDIF). In that situation, the established standard normally wins. (Remember Betamax vs VHS?) However, STEP is different because it has critical mass outside electronics. It is becoming more commercially important than EDIF and CFI can ever hope to become. As the market situation unfolds, STEP will be the dominant player, and EDIF and CFI will become isolated, unimportant historical artifacts. For many players, it will be smarter to use STEP, the complete, well-written and well-integrated standard with massive market support. Finally, since neither EDIF nor CFI has succeeded in gaining wide use, users can discard them without wasting too much investment.

Look for an example

What happens now depends on the major players within the user community. They should become well-informed of the business potential of aggressive use of standards. Any industry group could follow in the footsteps of the German automobile industry, for example. Those manufacturers created and funded the ProSTEP project to define a suitable AP and to develop the software to translate to and from the CAD systems they used. The manufacturers did not ask the permission of CAD vendors before taking this step. They simply decided to take control of their own data—with or without the help of the CAD vendors—so that they could build the information systems they wanted. Initially, the manufacturers did not even invite the CAD vendors to join them. Later, when the vendors did join the group, they provided support for that AP, the AP 214 Core Data for Automotive Mechanical Design Processes.

Finally, it is understandable if the people behind EDIF and CFI are not enamored of something that has "not invented here" written all over it and that is effectively going to put them out of business. However, this should not stop users from adopting STEP in electronics. Times change, and one technology generation replaces another. EDN

Author's biography

Lars Celander is a research scientist at the Institutet för Verkstadsteknisk Forskning (the Swedish Institute of Production Engineering Research), Mölndal, Sweden. He has worked at the company for five years, helping Swedish industry use the Standard for the Exchange of Product Model Data. Celander received an MSc in Engineering Physics from Chalmers University of Technology. In his spare time, he enjoys sailing, scuba diving, and watercolor painting.

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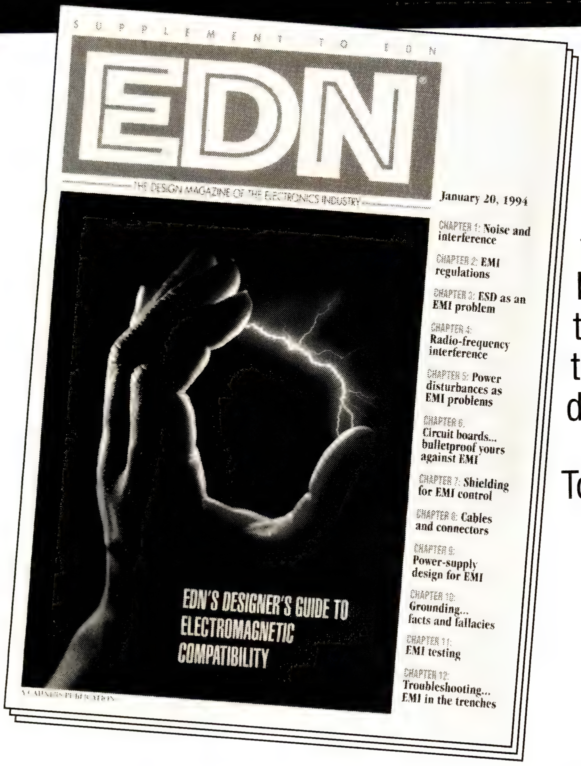
A NONTRADITIONAL APPROACH TO EMI



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January 20, 1994

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CHAPTER 2: EMI regulations

CHAPTER 3: ESD as an EMI problem

CHAPTER 4: Radio-frequency interference

CHAPTER 5: Power disturbances as EMI problems

CHAPTER 6: Circuit boards... bulletproof yours against EMI

CHAPTER 7: Shielding for EMI control

CHAPTER 8: Cables and connectors

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New switching diodes in ceramic surface-mount package

The SOD110, the first ceramic surface-mount package for diodes, is identical in size to industry-standard 0805 chip components.

Philips Semiconductors has introduced the world's first general-purpose switching diodes to be housed in a ceramic surface-mount package with the same pc board footprint as an industry-standard 0805 chip capacitor. The new SOD110 packages can be handled by pick-and-place equipment in the same way as 0805 capacitors and they are suitable for use with all current SMD soldering techniques.

The BAS216 and BA792 are the first in a complete family of diodes to be offered in the new package. Compared with plastic encapsulations, the superior thermal characteristics of the SOD110 ceramic package help to reduce junction temperatures, enhancin long-term reliability and permitting maximun power dissipations as high as 400 mW.

The BAS216 is a high-speed silicon epitaxial switching diode with repetitive peak forward current and continuous DC forward current ratings of 500 mA and 250 mA respectively. Its repetitive peak reverse voltage rating is 85 V and its maximum reverse recovery time is 6 ns. The second SOD110 device to be introduced, the BA792, is a band-switching diode; Schottky and zener diodes will follow shortly, with more additions scheduled.

For ease of handling and to ensure correct polarity during placement, the diodes are supplied in 8mm tape-on-reel packaging containing 3000 devices per reel.

Call 1-800-447-1500 Ext 5022
Europe: circle no. 40

Expanded range of industry-standard packages for discretes

The arguments for establishing second sources for many semiconductor devices are well appreciated. Second sourcing provides customers with the reassurance of continued supply, and it can also be favourable for manufacturers to cooperate in second sourcing, to help establish standards in a highly diverse market place.

Philips Semiconductors is responding to this trend with the launch of a new product range in the Japanese SC59/70 packages. The new devices are 100% electrically and mechanically equivalent to other manufacturers' devices, so no alterations to existing designs and placement routines are required, and the type numbers are the same, so that second sourcing is very simple.

With the release of the PNP 2PA and 2PB transistors and the NPN 2PC and 2PD transistors, Philips Semiconductors has a standard family of their existing small-signal general-purpose transistors in the Japanese SC59/70 packages. The transistors have a high DC current gain and low collector/emitter saturation voltage so are suitable for all general switching and amplification applications in the consumer, communications, computing, automotive, test and measurement and medical fields.

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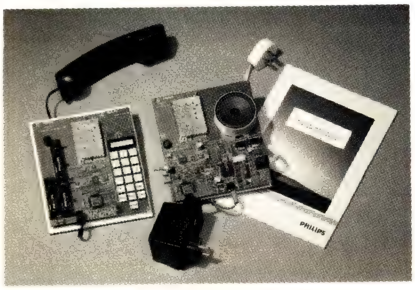
Philips
Semiconductors

Turnkey evaluation kits for complete 3 V CT1 and CT1+ solutions

New second generation turnkey evaluation kits have been introduced by Philips Semiconductors for their CT1 and CT1+ standard cordless telephone chipset. This 3 V solution is based on the know-how developed with the previous 5 V kit, and offers the same proven reliability, with enhanced performance.

These complete kits (OM4743 for CT1, OM4744 for CT1+) include a board, full software support and an RF transceiver, permitting fast turn-around times in developing competitive CT1 or CT1+ products. They allow low-risk development and help reduce time-consuming board design.



The turnkey evaluation kits for the 3 V CT1 and CT1+ standard chipset include full software support.

The chipset supports six handsets per base and numerous functions such as 2-way paging, 2-way intercom, call transfer and selective ringing. As a 3 V, low-current solution, board designs can now deliver longer talk time and more than 60 hours standby time from the three NiCd cells. Battery management features such as high and trickle charging ensure long battery life. The board also has an LCD display, a temporary switch for DTMF (data dialling) and a changeable security code. Voice scrambling is supported with the addition of one extra integrated circuit.

Parameters may be factory-configured and can be preset for CT1 or CT1+ operation, the number of channels (40 for CT1, 80 for CT1+), ID code exchange on/off and exchange time, DTMF burst/pause time and so on. The single microcontroller which covers all countries also has a Service and Production mode which can be used to set the configuration; this mode can also be used to test the set on the production line, or later in the service workshop.

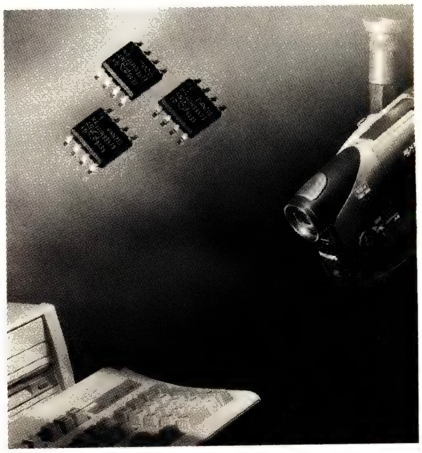
Call 1-800-447-1500 Ext 1178
Europe: circle no. 42

New low-ohmic MOSFETs for high-efficiency low-voltage switching

Philips Semiconductors' latest range of dual and single Vertical DMOSFETs offers state-of-the-art low-ohmic technology in the space-saving SO8 (SOT96) package. By improving the cell density of its existing V-DMOS process and combining that with its surface-mount expertise, Philips can now offer MOSFETs ideally suited for applications that have previously required the low resistance and high current capabilities of larger and more expensive devices.

Applications that can take advantage of the space and cost savings of small-signal surface-mount technology include DC motor drive/control (disk drives, printer motors, video camera motors, etc), battery management and power supply management. Dual low-ohmic MOSFETs provide efficient switching in the power management stage of these applications. Another key application is on the load side of an SMPS; used for synchronous rectification, these transistors can deliver overall SMPS efficiencies up to 90% for outputs less than 5 V.

The advanced self-aligned DMOS manufacturing process which realizes the high cell density in these transistors produces an extremely low $R_{DS\,(on)}/mm^2$ for this type of transistor. Additional benefits include true 3 V logic switching compatibility, high-speed switching and no secondary breakdown. Future developments will focus on an even lower $R_{DS\,(on)}$ (down to 0.05 Ω) and lower profile packages. The initial range is shown in the table.



New low-ohmic MOSFETs are ideal for DC motor drive/control in disk drives and video camera motors.

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Europe: circle no. 43

Type number	Resistance	Description	Package
PHN210	0.1 Ω	N channel dual FET	SO8
PHP225	0.25 Ω	P channel dual FET	SO8
PHC21025	0.1 Ω/0.25 Ω	N/P channel complementary pair	SO8
BSP100	0.1 Ω	N channel single FET	SOT223
BSP250	0.25 Ω	P channel single FET	SOT223

Low leakage current small-signal diodes in SOT23 package

With the introduction of the BAS116, BAV170, BAV199 and BAW156, Philips Semiconductors now offers a new range of small-signal diodes in the industry-standard SOT23 package. They complement Philips' popular BAS16, BAV70, BAV99 and BAW56 diode types.

The new diodes' low leakage current, with the resultant very low battery drain, makes them suitable for portable applications and products in which battery power must be maintained without use for periods of up to one month. They also have an extended reverse recovery time, providing transient suppression in noisy supply line environments.

These state-of-the-art diodes are ideal for high-volume applications including domestic appliances, cellular and cordless telephones, computer equipment such as PCs, modems and disk drives, and general test and measurement devices. They are also highly suitable for a range of functions in the automotive field.

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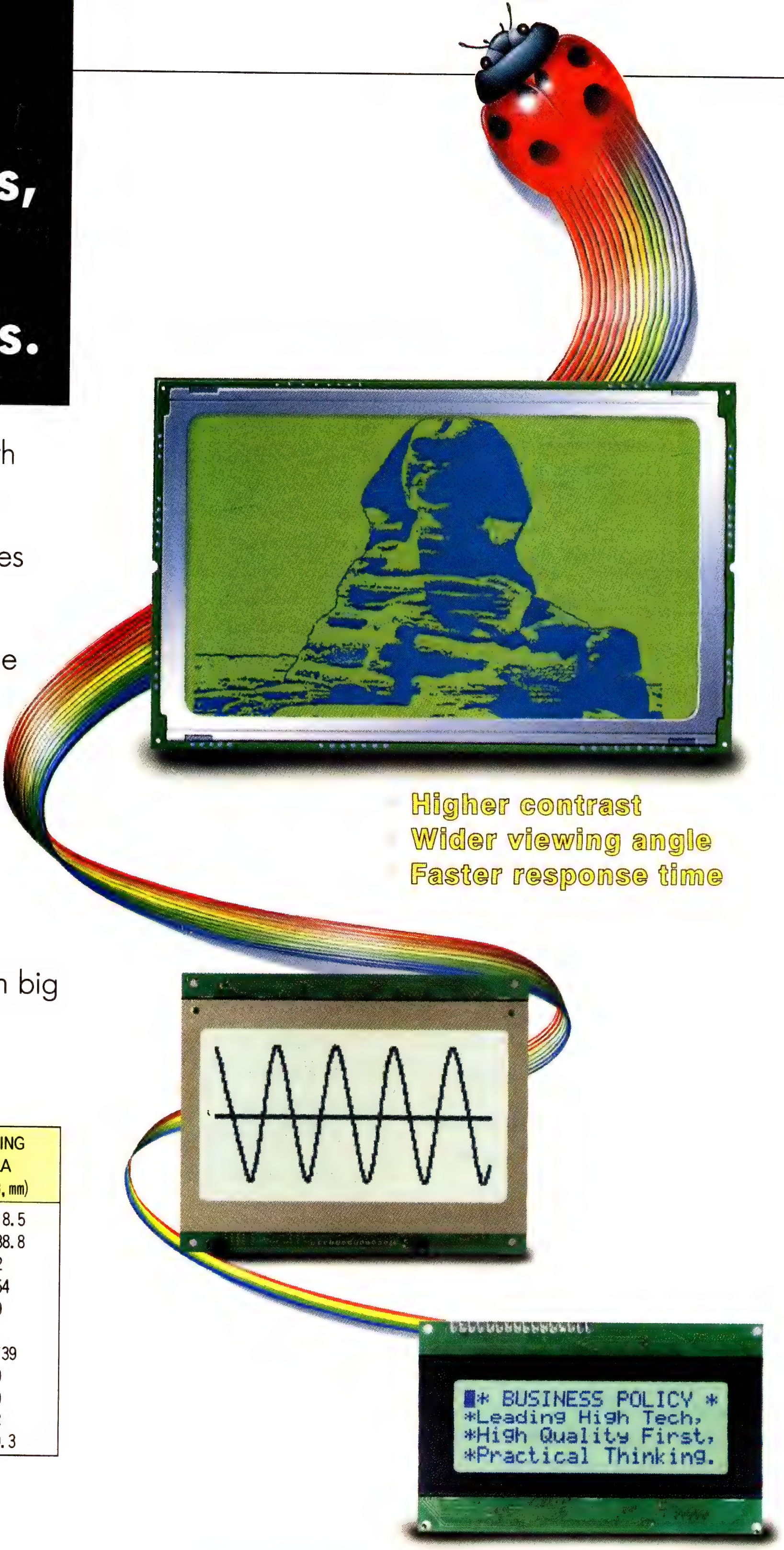

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HG12602	128×64	93×70×10	70.7×38.8
HG16501	160×128	129×102×11.5	101×82
HG19501	192×128	98×86×13	77.5×54
HG24501	240×64	180×65×11	132×39
HG24502	240×64	129×62×10	87×42
HG24503	240×64	180×65×10	132.6×39
HG25501	256×128	147×116×12	127×70
HG25601	256×128	147×116×12	127×70
HG32601	320×240	157×110×8.5	121×92
HG32602	320×240	143×96.8×9.5	104×79.3

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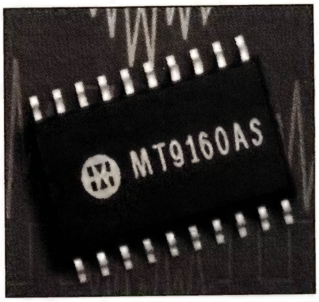
Fiber-optic transceiver chip set for 1063-Mbps fiber-channel and 622-Mbps Sonet applications. The MAX3260 high-speed transimpedance amplifier is useful in optical receivers with as much as 25 dB of input-signal range. The amplifier operates from a 5V supply and consumes 115 mW when ac coupled or 300 mW with 50Ω output terminations. The MAX3261 is a 1.2-Gbps laser-diode driver with complementary enable inputs for interfacing with open-fiber-control architecture. An automatic power-control circuit maintains constant power and requires a monitor photodiode. The MAX3262 high-gain, wide-bandwidth amplifier is useful as a postamplifier in fiber-optic receivers with data rates to 1 Gbps. You can adjust the gain between 33 and 48 dB. The amplifier provides chatter-free loss-of-signal detection with adjustable hysteresis. The devices are available in die form and start at $9.25 (100). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 443**

EPLD family reduces prices. The vendor has reduced the prices of the MAX 7000 family of EPLDs up to 57%. Some representative prices for the fastest speeds are $21.95 (100) for the 64-macrocell EPM7064-LC68-7, $32.95 (100) for the 96-macrocell EPM7096-LC68-7, $87.95 (100) for the 160-macrocell EPM7160-QC100-10, and $199.95 (100) for the 256-macrocell EPM7256ERC208-12. The EPM7064LC44-15 costs $6.95 (100). **Altera Corp**, San Jose, CA. (408) 894-7000. **Circle No. 444**



Codec includes filters, gain control, programmable sidetone path, and driver amplifier. The MT9160 multifeatured codec has a fully differential audio-path architecture, providing wide dynamic range and high noise rejection while operating from a single 5V supply. Its 300Ω driver eliminates the need for external amplifiers and allows direct interfacing to any digital phone handset receiver. The codec is available in 20-pin SOIC and 24-pin DIP packages and starts at $4.38 (10,000). **Mitel Semiconductor Corp**, Ontario, Canada. (613) 592-2122. **Circle No. 445**

ARINC 429 transceiver has four receive and two transmit channels. The DD-42900 has a 32-word×32-bit FIFO buffer for each transmit and receive channel, plus a 128×32-bit shared RAM interface. To simplify interfacing, the transceiver also has data-match and data-store processors that provide an intelligent interface between 8- and 16-bit processors and Aeronautical Radio Inc

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CIRCLE NO. 136

(ARINC) 429 data buses. The device comes in a 1×3-in. package and costs $250. **ILC Data Device Corp**, Bohemia, NY. (516) 567-5600.
Circle No. 446

Terminal-rate adapter circuit for ISDN. The 29C93A performs speed adaptation between synchronous and asynchronous V.24 terminals through 64-kbps integrated-services-digital-network (ISDN) B channels. The device supports the ECMA 102/V.110 protocol. Asynchronous data rates range from 50 bps to 57.6 kbps, and synchronous data rates range from 600 bps to 64 kbps. A PC evaluation package is available. $9.80 (5000). **Temic Telefunken Microelectronic GmbH**, Heilbronn, Germany. (+71 31) 67-29 45.
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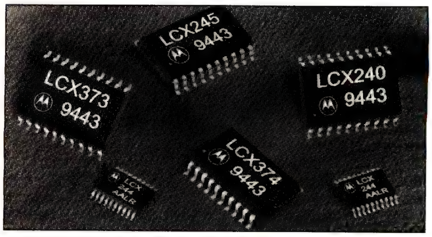

CMOS logic family interfaces to 3 and 5V devices. The MC74LCX logic family can interface to pure 3V or both 3 and 5V in the same design, without sacrificing performance. The devices operate from 2.7 to 3.6V supplies and have 10-µA current consumption in all three logic states. The low voltage and low-current operation substantially reduce power requirements over earlier logic families. The MC74LCX240, 244, 373, and 374 cost $1.11 (1000) and the 245 costs $1.41 (1000) for SOIC packages. The devices are available in TSSOP packages. **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 655-3397. **Circle No. 448**

Nonvolatile serial ferroelectric RAMs offer low read current and 10 billion write cycles. A 16-kbit FM24CZ16 serial memory with I^2C bus has an active current of 250 µA and a standby current of 1 µA. The device costs $1.43 (10,000). The 16-kbit FM25160 is compatible with the SPI bus and has an active current of 1.5 mA and a standby current of 5 µA over the commercial temperature range and 10 µA over the industrial temperature range. The SPI bus device operates at 2.1 MHz and costs $1.61 (10,000). The serial memories are plug-in-compatible with EEPROM devices having similar part numbers. Other members of the product family include 4- and 8-kbit devices. **Ramtron International Corp**, Colorado Springs, CO. (719) 481-7000.
Circle No. 449

Single-chip spread-spectrum-transceiver IC. The S20043 can send and receive data at rates of 100 bps to 2 Mbps with direct sequence chipping rates up to 63 MHz. The transceiver behaves as an intelligent radio-peripheral device to a microcontroller. Interface is through a common address and data bus. The controller monitors the airwaves and customizes the characteristics of the radio's transmit and receive channels to best use the available spectrum. The programmable IC accommo-

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DS-186 In-Circuit Emulator

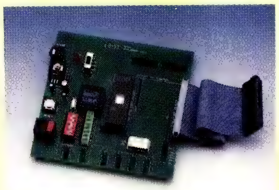
DS-186 real-time emulator supports microprocessors of the 80C186 family. The emulated devices are 80C186/8/XL/EA/EB/EC, V40/50, 8086/8 and more. The selection of a different microprocessor is made by replacing the microprocessor in the adapter or changing the adapter. The system features Full Speed Emulation up to 30MHz, 1 Mbytes of Zero Wait-State Mapped Memory, 8K Frames Dynamic Trace Buffer, 1M Hardware Breakpoints and 115KBaud RS-232C Communication Link. Breakpoints are qualified by instruction fetch, instruction execution, data contents, read/write from/to memory and I/O. The Trace display shows source, assembler and bus cycles. The system runs at the frequency of the crystal on the adapter or from the clock source supplied by the user hardware. The software supplied as standard is Paradigm Debug and Locate.

DS-51 Microprocessor Development System

Ceibo DS-51 is a real-time in-circuit emulator dedicated to the 8051 family of microcontrollers. It is serially linked to an IBM PC or compatible host and carries out a transparent emulation on the target microcontroller. DS-51 supports the new low-power and low-voltage 8051 microcontrollers and derivatives. The system can emulate the microcontrollers using either the built-in 5V power supply or any voltage applied to the target circuitry. This selection is done by means of software control. The permitted voltage range is from 1.5V to 6V or higher. DS-51 emulates almost every 8051 derivative in the complete voltage and frequency range specified by the microcontroller manufacturer. The minimum frequency is determined by the emulated chip characteristics, while maximum frequency is up to 40MHz. The software includes Source Level Debugger for PLM and C, Assembler Debugger, Performance Analyzer, On-line Assembler and Disassembler, Conditional Breakpoints and many other features. Standard systems are supplied with 128KBytes of Internal Memory, 64K Hardware Breakpoints, 32K Real-Time Trace Memory and personality probe supporting most of the 80C51 microcontrollers.

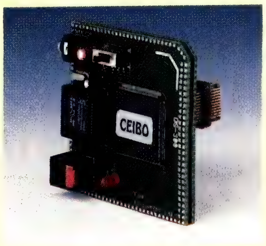
Development Tools

Ceibo offers a broad line of dedicated Development Tools for emulating different Microcontrollers and including all the necessary elements to design your embedded system. Among these tools are DB-51, DB-501, EB-51, DS-750 and DS-752.



DS-300 PSD Emulator

DS-300 is a complete software and hardware development tool that allows file generation and emulation of the PSD-3xx devices. The emulator provides an immediate way to check that the devices are properly configured and allows examination and modification of the memories and I/O lines. The configuration software provides all the elements necessary to set the device with minimum learning time.



MP-51 - Programmer

Ceibo MP-51 is a high-quality Microcontroller, Flash Memory, EPROM and PLD Programmer dedicated to all the microcontrollers belonging to the 8051 family, 24 to 32-pin EPROMs, high-density PLDs and PSD devices. MP-51 allows to enable or disable the PLD or Microcontroller security capabilities and handles Lock Bits and Encryption Table available in several Microcontrollers. MP-51 loads different file formats: Intel Hex, Intel OMF, Binary, Motorola S-records, etc. Adapters are available for all the possible packages, such as DIP, LCC, PLCC, SO, and QFP.

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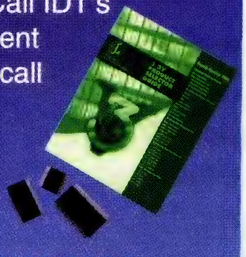

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2K × 9 FIFO	25ns
4K × 9 FIFO	25ns
8K × 9 FIFO	25ns

Integrated Device Technology, Inc.

dates a wide variation of direct-sequence, pseudorandom noise codes in lengths from 3 to 2047. The baseband IC can control digital data transmission in various bands. The device is targeted for the ISM bands at 915 MHz, 2.4 GHz, and 5.725 GHz and costs \$23.50 (10,000). **American Microsystems Inc**, Pocatello, ID. (208) 233-4690. **Circle No. 450**

Serial digital cable drivers have 400-Mbit/sec data rate. The CLC006 and CLC007 cable drivers conform to the SMPTE 259M standard for the transmission of Serial Digital Video Signals (144 Mbits/sec NTSC, 173 Mbits/sec Serial Digital Component, and 360 Mbits/sec Widescreen Component). The devices accept single-ended or differential ECL inputs and drive single-ended ac-coupled back-matched 75Ω video loads. The devices offer 650-psec rise and fall times and 1-nsec propagation delay. The CLC006 \$5.50 (1000) has two amplitude-adjustable outputs providing voltage swings from 370 mV to 1.07V p-p with a 75Ω load. The CLC007 \$4.75 (1000) drives fixed-ECL levels (800 mV p-p) over four back-matched 75Ω loads. Each device operates from 5V and –5 or –5.2V. Quiescent power consumption is 200 mW. **Comlinear Corp**, Fort Collins, CO. (303) 226-0500. **Circle No. 451**

Multistandard IR transceiver IC implements new IrDA standard. The CS8130 implements the Infrared Data Association (IrDA) standard providing cordless communication for mobile computer users. The standard overcomes the problem of proprietary IR interfaces that don't communicate with equipment from other manufacturers. The chip connects to a standard UART on one side and an LED and PIN diode on the other side. It transfers data in half- or full-duplex mode at rates from 2400 bps to 115.2 kbps. The 20-pin SSOP costs \$5.50 (1000). **Crystal Semiconductor Corp**, Austin, TX. (512) 422-7555. **Circle No. 452**

IR receiver building block provides complete preamp and comparators for data rates to 4 Mbps. The LT1319 converts modulated photodiode signals back to digital signals for wireless applications in computer systems at distances up to 2m. The chip supports low-speed standards, such as IRDA and Sharp/Newton, plus emerging standards with data rates above 1 Mbps. An 8-MHz bandwidth preamp with a transimpedance gain of 15 kΩ converts the current from an external photodiode to a voltage. The chip accommodates a variety of filtering schemes and provides 25- and 60-nsec comparators with adjustable thresholds for generating the final data outputs. A shutdown feature reduces the 14-mA current consumption to 500 μA. The device costs \$3.80 (1000) in a 16-lead SOIC package. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 453**

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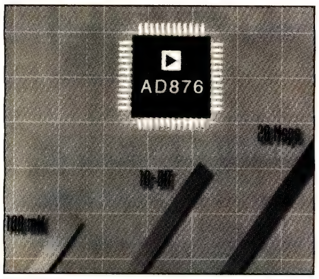


Video ADC converts 20M samples/sec with 10-bit resolution. The AD876 draws only 160 mW from a single 5V supply and includes a differential input track-and-hold amplifier, eliminating the need for external buffering. Digital error correction allows immediate sampling of the input without waiting for internal calibration. In a 28-pin SOIC or 48-lead TQFP, the device costs $9.95 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428. **Circle No. 383**

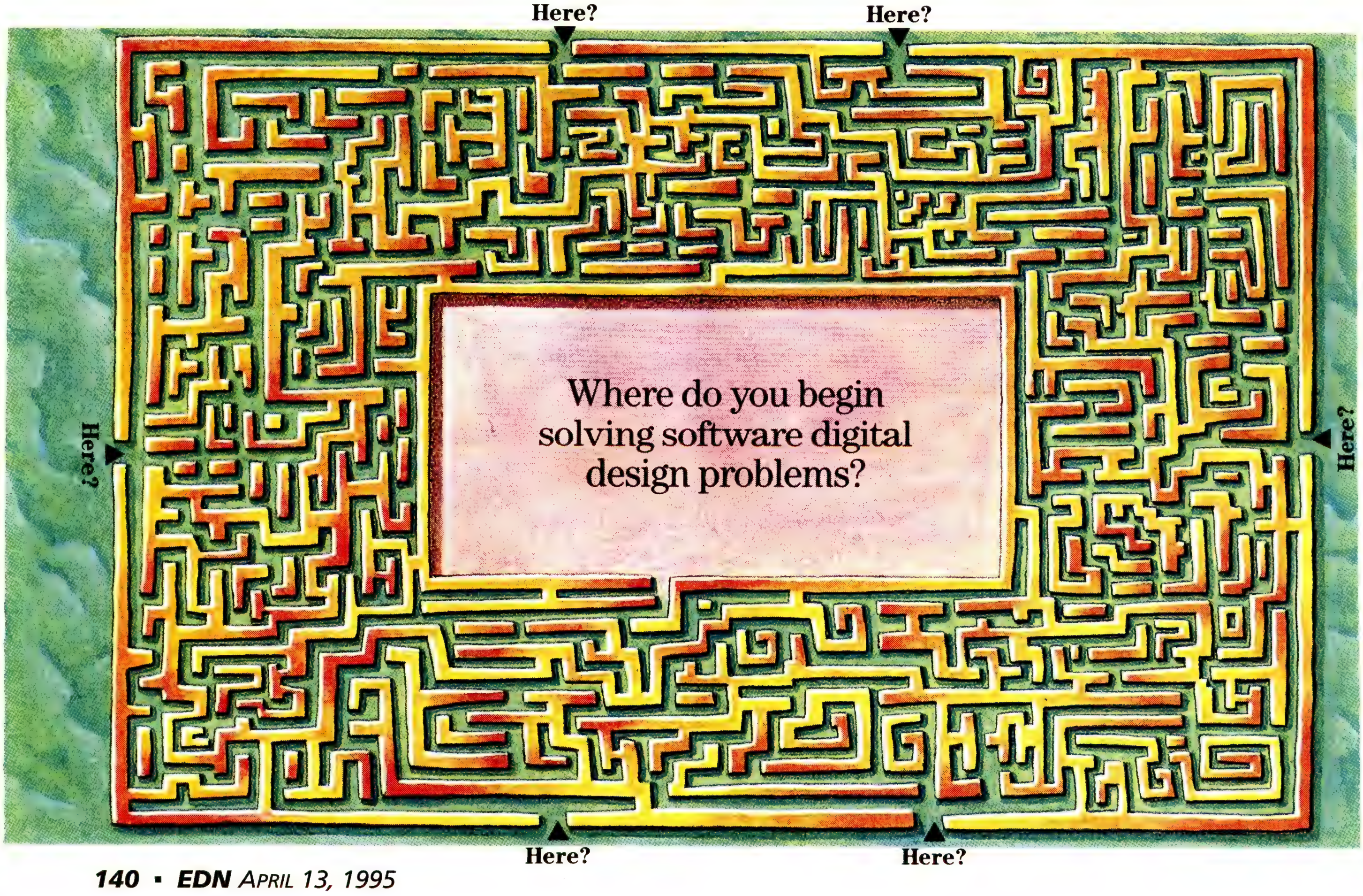
16- and 4-Mbit DRAMs offer 20-nsec EDO hyperpage-mode cycle and 50-nsec access times. These extended-data-out (EDO) DRAMs are also available in 25-nsec hyperpage-mode cycle and 60-nsec access time. The 1M×16-bit M5M-4V18165B has a 1-kHz refresh rate, and the M5M-4V16165B has a 4-kHz refresh rate. Both devices have a 540-mW power consumption and a 500-μA max standby battery-backup current. The 256k×16-bit M5M44265C has a 512-Hz refresh rate, a 650-mW power consumption, and a 150-μW max standby current. The 16-Mbit devices are available in 400-mil, 42-pin SOJ packages for $55 (1000) and 400-mil, 50-pin TSOP packages for $66 (1000). The 4-Mbit device costs $17 (1000) in SOJ packages and $17.50 (1000) in TSOP packages. Samples are available now, and production is scheduled for the third quarter. **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900.

Circle No. 384

Cache RAM offers 9-nsec access time and burst-mode operation for zero wait state with 100-MHz Pentium. The IDT71420 synchronous burst Cache RAM has a 32k×18-bit organization for zero-wait-state, secondary-cache applications with the fastest Pentium processors. The burst-mode function provides four address cycles of data with each address presented to the CacheRAM. The burst-mode operation allows the CacheRAM to outperform SRAMs in secondary-cache applications. An address-pipeline feature further improves performance, reducing clock cycles after the initial address access. Available in a 52-pin PLCC, the 9-nsec version of the 3.3V device costs $30 (10,000). **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345-7015.

Circle No. 385

PLL/frequency-synthesizer IC for analog cellular phones operates on low current. Operating from a 2.7 to 5.5V supply, the HD15501AT draws 100 μA in standby mode and 6 mA typ when operating. It has an internal prescaler and requires only an external loop filter and VCO to form a complete PLL synthesizer system. The prescaler has a minimum operating frequency of 1.1 GHz. You can set the division mode to 64/65 or 128/129 with a ser-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ial input switch. The device comes in a 20-pin TSOP and costs $2.95 (10,000). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 06.

Circle No. 386

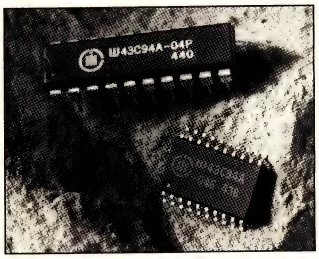
Two-channel current-mode controllers provide synchronized voltage output. The CS-3865C has a start-up voltage of 14V, and the CS-3865X has a start-up voltage of 8.4V. Both chips contain dual PWM output drivers that can source or sink up to 1A. The drivers operate at a 50% nominal duty cycle and are synchronized 180° out of phase to prevent cross-conduction problems in push-pull stages. The fixed-frequency current-mode controllers operate at clock frequencies up to 500 kHz. An on-chip oscillator controls both PWM output drivers. In 16-lead DIP or SO packages, the CS-3865X costs $1.13 (10,000), and the CS-3865C costs $1.06 (10,000). **Cherry Semiconductor Corp**, East Greenwich, RI. (401) 885-3600.

Circle No. 387

PCMCIA flash-memory-card evaluation kit. The PCMCIA flash-memory-card evaluation kit provides a tool for evaluating the company's C-Series flash-memory card. The kit includes a 1-Mbyte C-series flash-memory card, a user's guide, an SCM SwapBox Lite PCMCIA-card drive, an SCM-FTL flash-file system, Award CardWare 2.0 software, the Datalight CardTrick FFS/FTL flash-file system, and SystemSoft CardSoft+. The kit requires a PC with an ISA slot and costs $199. **Advanced Micro Devices Inc**, Sunnyvale, CA. (408) 749-5703.

Circle No. 388

Serially programmable graphics clock chip operates from 8.75 to 135 MHz. The W43C94A dual-output, programmable graphics clock generator uses a dual-PLL frequency synthesizer. The device comes with 16 video-clock frequencies and four or eight memory-clock frequencies preprogrammed in ROM. You can mask-program or individually program custom frequencies with a 20-bit serial data word. The device draws 25 mA from a 5V supply, dropping to 30 μA in power-down mode. Available in a 20-pin DIP or SOIC package, the device costs $2.70 (5000). **IC Works Inc**, San Jose, CA. (408) 922-0202.



Circle No. 389

1-Mbit synchronous SRAM for Pentium and PowerPC has 8-nsec access time. The 32k×32-bit TC55V1325FF and the 64k× 16-bit TC55V1165FF synchronous SRAMs support Pentium and PowerPC systems at bus frequencies up to 66 MHz. The architecture enables continuous data output resulting in faster data transfers. A 2-bit burst counter supports the Pentium burst and linear burst sequences. Both of the 3.3V devices use a self-timed write

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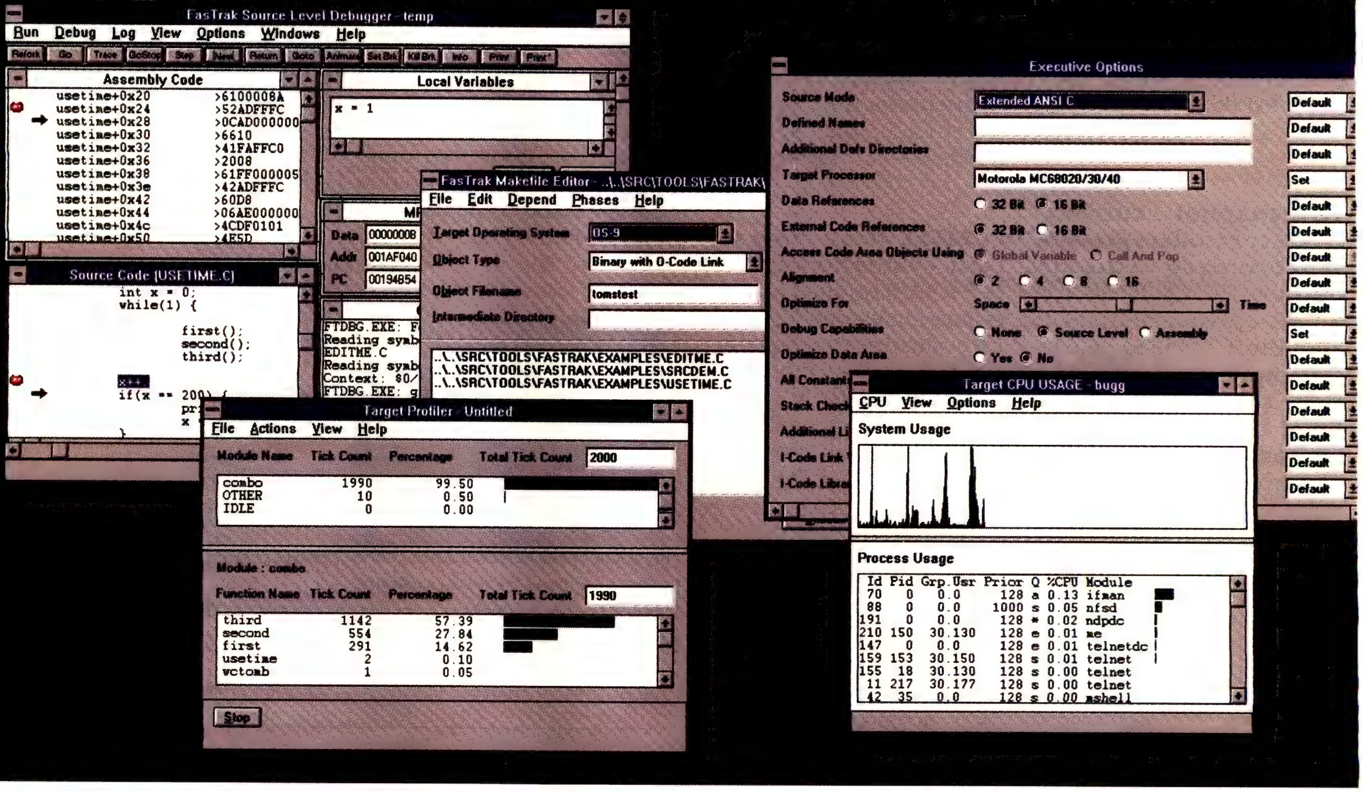
Your Window to OS-9 Real-Time Development


FasTrak Source Level Debugger - temp
Run Debug Log View Options Windows Help
Refork Go Trace GoStop Step Next Return Goto Animate Set Brk Kill Brk Info Print Prev
Assembly Code
Local Variables
Source Code (USETIME.C)
MP
FasTrak Makefile Editor - ..\..\SRC\TOOLS\FASTRAK\
File Edit Depend Phases Help
Target Profiler - Untitled
File Actions View Help
Stop
Executive Options
Target CPU USAGE - bugg
CPU View Options Help
System Usage
Process Usage

```
usetime+0x20        >6100008A
usetime+0x24        >52ADFFFC
usetime+0x28        >0CAD000000
usetime+0x30        >6610
usetime+0x32        >41FAFFC0
usetime+0x36        >2008
usetime+0x38        >61FF000005
usetime+0x3e        >42ADFFFC
usetime+0x42        >60D8
usetime+0x44        >06AE000000
usetime+0x4c        >4CDF0101
usetime+0x50        >4E5D
```

```
x = 1
```

Data 00000008
Addr 001AF040
PC 00194854

```
        int x = 0;
        while(1) {

                first();
                second();
                third();

        x++;
        if(x == 200) {
                pr
                x

        }
```

```
FTDBG.EXE: F
Reading symb
EDITME.C
Reading symb
Context: $0/
FTDBG.EXE: g
```

Target Operating System: OS-9
Object Type: Binary with O-Code Link
Object Filename: tomstest
Intermediate Directory:

```
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\EDITME.C
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\SRCDEM.C
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\USETIME.C
```

```
Module Name   Tick Count   Percentage   Total Tick Count  2000

combo             1990        99.50
OTHER               10         0.50
IDLE                 0         0.00

Module : combo

Function Name  Tick Count  Percentage   Total Tick Count  1990

third             1142        57.39
second             554        27.84
first              291        14.62
usetime              2         0.10
wctomb               1         0.05
```

Source Mode: Extended ANSI C — Default
Defined Names: — Default
Additional Defs Directories: — Default
Target Processor: Motorola MC68020/30/40 — Set
Data References: ○ 32 Bit ● 16 Bit — Default
External Code References: ● 32 Bit ○ 16 Bit — Default
Access Code Area Objects Using: ● Global Variable ○ Call And Pop — Default
Alignment: ● 2 ○ 4 ○ 8 ○ 16 — Default
Optimize For: Space … Time — Default
Debug Capabilities: ○ None ● Source Level ○ Assembly — Set
Optimize Data Area: ○ Yes ● No — Default
All Constant — Default
Stack Check — Default
Additional Li — Default
I-Code Link — Default
I-Code Libra — Default

```
 Id Pid Grp.Usr Prior Q %CPU Module
 70   0   0.0     128 a 0.13 ifman
 88   0   0.0    1000 s 0.05 nfsd
191   0   0.0     128 * 0.02 ndpdc
210 150  30.130   128 e 0.01 me
147   0   0.0     128 e 0.01 telnetdc
159 153  30.150   128 s 0.01 telnet
155  18  30.130   128 s 0.00 telnet
 11 217  30.177   128 s 0.00 telnet
 42  35   0.0     128 s 0.00 mshell
```

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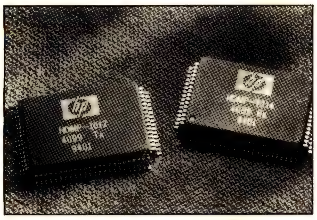
CIRCLE NO. 159

circuit to generate the internal pulse for a write operation. Each input and output circuit provides a temporary one-cycle data-storage register. Available in a low-profile QFP, samples cost $37 for the 8-nsec version, $32 for the 10-nsec version, and $26 for the 12-nsec version. Samples will be available in the second quarter, and volume production will begin in June. **Toshiba America Electronic Components Inc**, Irvine, CA. (800) 879-4963.

Circle No. 390

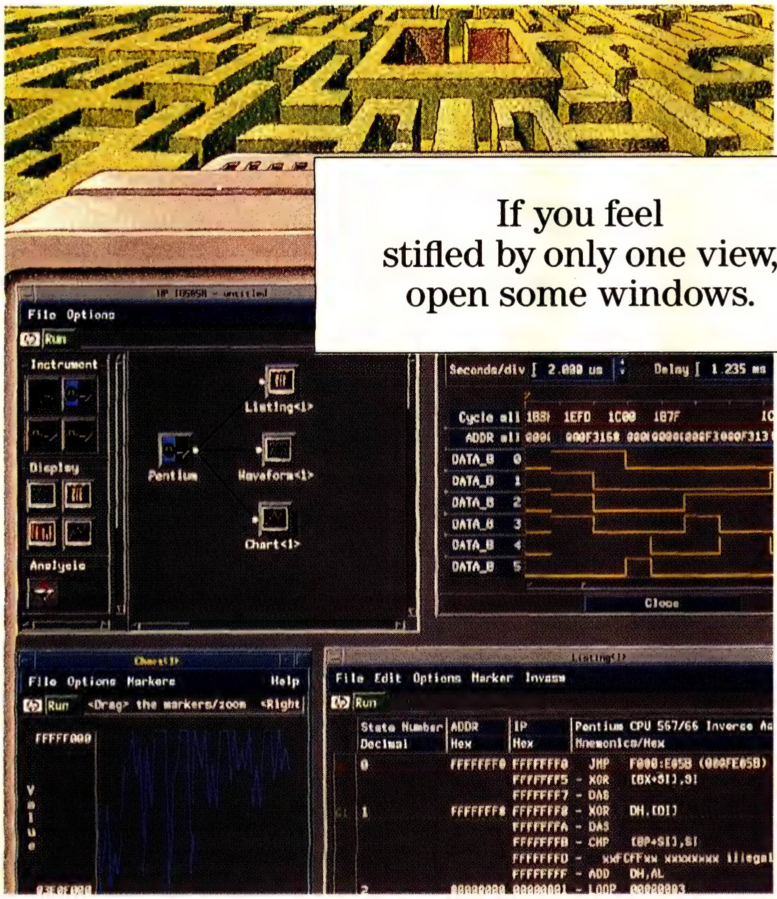
12×12-bit alpha mixer performs precise cross fades in real time. The LF48212 DSP chip mixes two video signals by blending them according to a pre-established alpha-mix formula in real time. The chip includes two multipliers, a summer, and all internal circuitry to generate the one-minus-alpha weighting for blending. The device comes in 68-pin PLCCs and 64-pin PQFPs, and prices start at $56 (100). **Logic Devices Inc**, Sunnyvale, CA. (408) 737-3300. **Circle No. 391**



Serial-link chip set provides 1.5-Gbps data rates in M-quad 80 aluminum package. The HDMP-1012 transmitter costs $90.05 (10), and the HDMP-1014 receiver costs $90.05 (10). The chips are bus and backplane extenders for video distribution. The serial link can be up to 20m with coaxial cable. Longer distances require fiber-optic modules. The transmitter accepts unrestricted serial data of 16, 17, 20, or 21 bits. Standard multiplexing/demultiplexing ICs let you use a double-frame mode to transmit 32- or 40-bit-wide data. The chips perform the encoding and decoding, multiplexing and demultiplexing, clock generation, clock and data recovery, and bit and frame synchronization. In duplex mode, the chips also provide link-start-up and -maintenance. **Hewlett-Packard Co**, Santa Clara, CA. (800) 537-7715, ext 9094.

Circle No. 392

Two-chip set provides kernel processor and vocoder for low-power GSM station. The VP22002 kernel processor and VP22020 vocoder perform the baseband signal processing for a Global System for Mobile (GSM) station. The chips comply with all GSM specifications and provide all processing from speech vocoding through the radio-system modular interface. The kernel processor provides the channel coder, equalizer, Gaussian-filtered-minimum-shift-keying modulator and timing generator, and a 32-bit ARM RISC microcontroller. The chip set draws 155 mW at 5V in active mode, 25 mW in idle mode, and 10 μW in sleep mode. In a 176-pin TQFP, the device costs $47 (1000). The vocoder features 13-kbps operation, asynchronous coding and decoding, two asynchronous data ports, and a host μP interface. It draws 85 mW at 5V in active mode and 0.1 mW in sleep mode. In a 100-pin TQFP, the vocoder costs $18 (1000). **VLSI Technology Inc**, San Jose, CA. (408) 434-3000. **Circle No. 393**



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CIRCLE NO. 121

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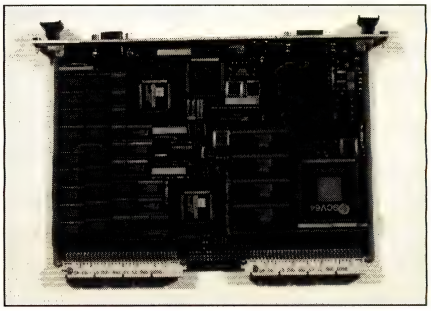
VMEbus DSP board offers eight 50-MHz TMS320C40 DSPs with MIXbus or PCI local bus. The model 4285 VME board is aimed at compute-intensive applications such as speech, radar, sonar, digital filtering, medical and industrial imaging, telecommunications, and military/aerospace. The board has a VME64 master/slave interface and a P2 interface that you can use for VSBus or custom I/O. Mezzanine interfaces include the modular-interface-extension (MIX) modules and PCI-Mezzanine-Card (PMC) modules using the PCI local bus. The board features 1 Mbyte of global SRAM and 1 Mbyte of local SRAM for each processor. The 6U VME board costs approximately $20,000, depending on configuration. **Pentek Inc**, Norwood, NJ. (201) 767-7100. **Circle No. 430**

Stand-alone emulator supports Ada debugger. The Mountain-510/WS universal DSP emulator card combined with the AdaScope debugger from Tartan (Pittsburgh, PA) supports Ada development for TI TMS320C3x and TMS320C4x DSPs. The SBus emulation card costs $4995. **White Mountain DSP Inc**, Nashua, NH. (603) 883-2430. **Circle No. 431**



68040-based VMEbus single-board computer accommodates up to 64 Mbytes of DRAM. The SVME/DMV-163 is designed for commercial, rugged, and military VME applications. It has two serial ports, a real-time clock calendar, and a 16-bit counter/timer; the SBC accommodates up to 4 Mbytes of flash EPROM. The board uses the company's proprietary MAXPack mezzanine module system to augment the functionality of the base board with I/O, memory, or custom data-acquisition modules. The modules are available in both air-cooled and conduction-cooled versions. Modules available for the board include the MAX-654 with dual redundant 1553B interfaces; the MAX-651 with a single 1553B interface, two RS232C/422 serial channels and nonvolatile memory; and the MAX-220 intelligent I/O processing subsystem providing Ethernet, SCSI, four serial ports, and a parallel interface. The SVME/DMV-163 starts at $7528. **DY 4 Systems Ltd**, Campbell, CA. (408) 377-9822. **Circle No. 432**

In-circuit emulator for 8031, 8032, 8051, and 8x52 microcontrollers. The NICE-52 in-circuit emulator comes with 64k words of code memory, 64k words of data memory, and a 40-pin

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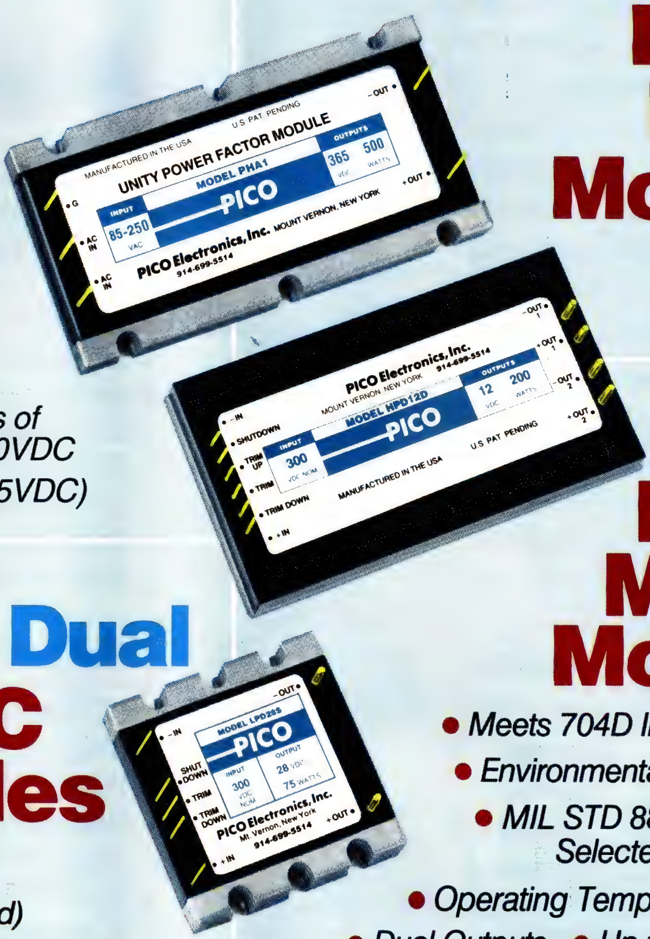

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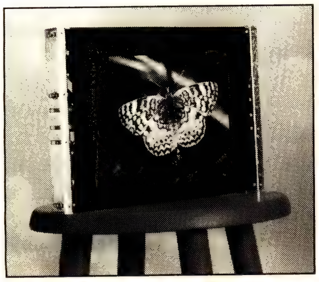
DIP connector to connect your target board. An ISA bus interface connects to PCs. The unit runs in real-time up to 16 MHz, and you can use it without a target for preliminary software debugging. $895. **Tribal Microsystems Inc**, Fremont, CA. (510) 623-8859.
Circle No. 433

Pentium-processor probe for logic-analysis system lets you control execution. The E3491A Pentium-processor probe ($7500) works with the HP 16505A prototype analyzer ($4995) and an HP 16500B logic-analysis-system mainframe ($8980). The probe lets you start and stop code execution on the system under test, simplifying troubleshooting and debugging. The probe provides access to the Pentium's registers and memory, and the logic analyzer lets you view external data and buses, giving you a complete picture of a system's operation. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9183. **Circle No. 434**



486-based flat-panel computer has sunlight-readable active matrix monochrome display. The DisplayPac-SunVue flat-panel computer offers a local bus video controller with built-in Windows accelerator, up to 32 Mbytes of DRAM, a 1.5-Mbyte solid-state disk, hard-disk interface, and floppy-disk interface. The touch-sensitive CCFT edgelit display measures 9.5 in. diagonally and offers 640×480-pixel resolution with 256 gray levels. The complete computer measures 12.5×8.5×3 in. With a 25-MHz 486SX, the computer costs $3195 (OEM qty). **Computer Dynamics**, Greer, SC. (803) 877-8700.
Circle No. 435

Motherboards based on the 75-MHz SuperSPARC-II offer high performance for embedded systems. The 75-MHz SPARCengine 20-71 motherboard provides 125.8 SPECint92 and 121.0 SPEfp92 operation. The motherboards are compatible with existing SPARCstation 10 and 20 workstation hardware and require no application or operating-system changes. The boards are binary-compatible with software developed for the SPARC platform. You can add a second processor module for increased performance. The motherboard with one SuperSPARC-II module and a Solaris right-to-use license costs $10,300 (one) and $9700 without the Solaris license. The 75-MHz SuperSPARC-II processor modules cost $2410 (1000). **Sun Microsystems Inc**, Mountain View, CA. (415) 960-1300. **Circle No. 436**

Virtual-device-driver tool kit for C and C++ works with Windows for Workgroups 3.11. VtoolsD version 1.1 supports the advanced driver architecture of Windows for Workgroups 3.11 and includes support

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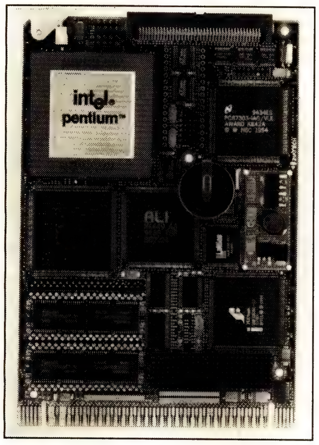
CIRCLE NO. 186

for Borland's 32-bit C++ compiler. According to the company, Windows 95 will have much of the same operating-system technology as Windows for Workgroups 3.11, allowing you to get a head start on Windows 95 programming. The software costs $495. **Vireo Software Inc**, Bolton, MA. (508) 779-8352. **Circle No. 437**

PC-to-host communication software provides OLE 2 automation support. Pipeline 2 acts as a universal communication hub for mixed platforms and operating systems, networks, modems, and serial lines. The software lets you simultaneously access up to 16 applications from a variety of host computers and move data between the applications. To use the software, you write client programs in Visual Basic, Visual C++, or any other object-linking-and-embedding-2-compatible language. $395. **Falco Data Products Inc**, Sunnyvale, CA. (408) 745-7123. **Circle No. 438**



100-MHz Pentium computer board for STD 32 bus has PCI expansion. The ZT 8905 single-board computer provides PCI expansion through a small-form-factor mezzanine board. The SBC features DOS in flash memory, 8- to 48-Mbyte DRAM, 2 to 4 Mbytes of flash memory for embedded programs, two serial ports, an EPP/ECP-capable parallel port, and a keyboard controller. An IDE hard disk is optional. With a 100-MHz Pentium, 2 Mbytes of flash memory, and 8 Mbytes of DRAM, the 4.5×6.5-in. board costs $2935. **Ziatech Corp**, San Luis Obispo, CA. (805) 541-0488. **Circle No. 439**

CPU boards for VMEbus offer 68040 and 68060 CPUs with 68360 communications controller. The 33-MHz 68040-based Nitro 240 ($5195) and the 50/66-MHz 68060-based Nitro 260 ($5695) suit high-performance, real-time, embedded applications, such as video on demand, communications, high-speed printing, image processing, and real-time simulation. The board has a 64-bit VME64 system-bus interface, and the 68360 provides four 2.048-Mbps serial communications channels. Other features include an 80-Mbyte/sec Corebus mezzanine/local-bus interface, an Ethernet interface, SCSI-II interfaces with DMA, and two additional front-panel serial I/O ports. The board accommodates up to 64 Mbytes of DRAM, 512 kbytes of EPROM, 2 kbytes of nonvolatile RAM, and up to 4 Mbytes of flash memory. The prices include 8 Mbytes of DRAM. **Heurikon Corp**, Madison, WI. (608) 831-0900. **Circle No. 440**

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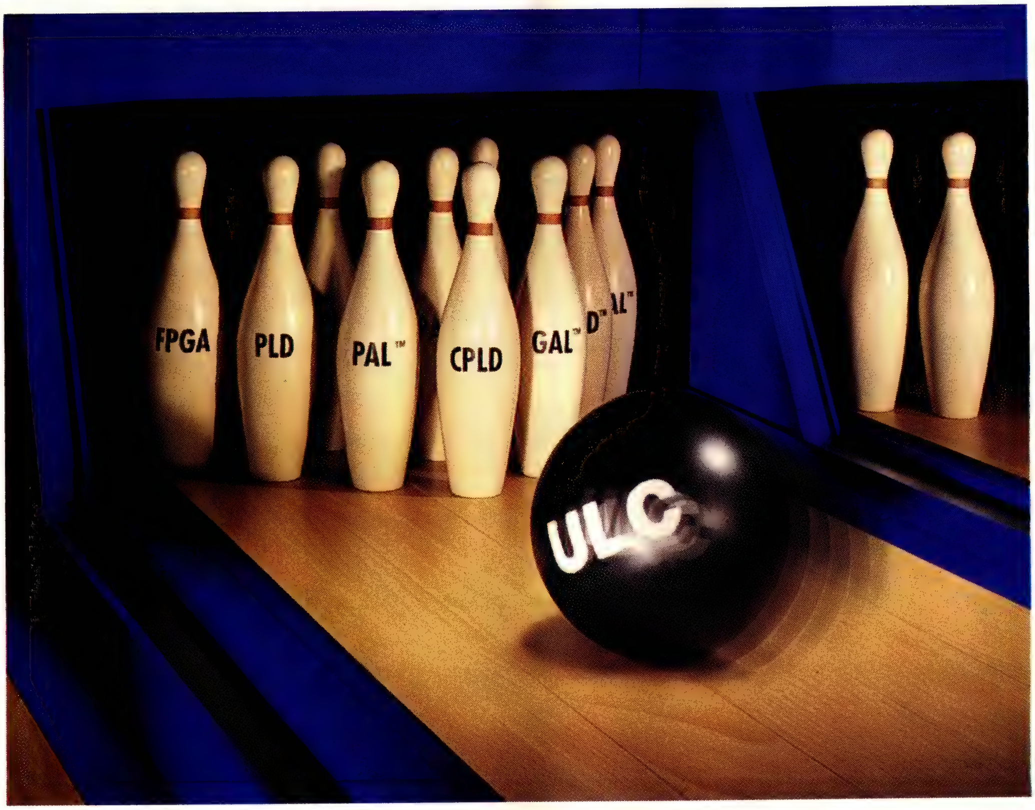

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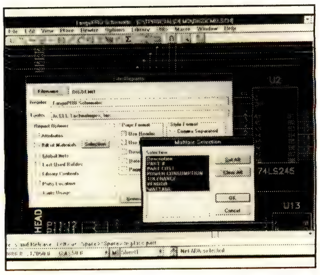
New release of FPGA design tool available in three versions for five FPGA suppliers. FPGA Foundry release 7 starts in the Access version for $995 on PCs. Access provides timing-driven design for FPGAs up to 3000 gates from any one of five FPGA suppliers. An all-vendor version of Access costs $2995 on PCs. FPGA suppliers covered include Actel, AT&T, Motorola, Texas Instruments, and Xilinx. The Catalyst version is available in single-, two-, and all-vendor configurations; it costs from $4995 to $9995. Release 7 supports devices up to 15,000 gates. FPGA Foundry Paragon costs $49,995 and provides all-vendor high-density FPGA design. The software includes timing-driven FPGA design, multiple-CAE-vendor integration kits, a floorplanner, and ASIC migration capability. The software handles FPGA prototyping of large ASIC designs. All of the tools are available on workstations. **NeoCAD**, Boulder, CO. (303) 442-9121. **Circle No. 348**



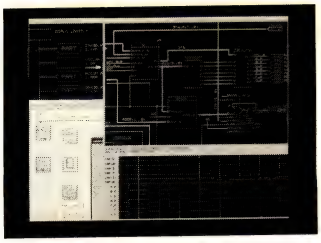
Schematic-capture tool adds streamlined net naming and custom bill of materials. TangoPRO Schematic Version 2.6 automatically names nets during placement, allowing you to insert consecutive wires efficiently without requiring a default name before the program accepts changes. The tool also automatically generates unique names when copying wires or splitting nets. You can customize the bill of materials by selecting the attributes you want to include in a report. The Windows-based tool costs $995. **Accel Technologies Inc**, San Diego, CA. (619) 554-1000. **Circle No. 349**

Simulation model for the 32-bit extension of the PCMCIA 2.0 specification. The CardBus standard includes both the new 32-bit extension and the original 16-bit (Classic) specification. The PC Card bus-interface model comprises five modules: CardBus master, CardBus slave, Classic master (host), Classic slave (card), and CardBus monitor/protocol checker. The model supports all key operational cycles, including read/write transactions, master-initiated terminations, target-initiated terminations, address/data stepping, interrupt handling, memory write and invalid date, and postable memory write. A perpetual site license costs $15,000. A comprehensive test suite, CardBus Test Suite, is also available for $5000. **Logic Modeling Group, Synopsys Inc**, Beaverton, OR. (800) 346-6335. **Circle No. 350**

Analog and mixed-signal HDL based on publicly available program. The Code Model Software Development Kit (CM-SDK) is based on the Unix-based XSpice program distributed by Georgia Tech Research Corp, a unit of the Georgia Institute of Technology. According to the company, the product is the only nonproprietary analog and mixed-signal hardware-description language (HDL) for Windows. The software lets you create Spice models using C subroutines, simplifying the creation of mixed-mode circuits, sampled data systems, and mixed domain (electrical-physical) descriptions. You can make the models as simple or as complex as you want. The software costs $3500 and is available bundled with the company's ICAP/4Windows simulator for $5500. **Intusoft**, San Pedro, CA. (310) 833-0710. **Circle No. 351**

Windows-based schematic-entry package costs $199 for competitive upgrades. The Schematics for Windows design package provides a symbol library of >32,000 components, supports unlimited levels of hierarchy in designs, integrated symbol and package editing, an unlimited number of pages per schematic and schematics per design, bill-of-material reporting, and backward-engineering-change-order support. The software lets you view multiple windows of the same or different schematics simultaneously. It can generate pc-board-layout netlist formats for Accel TangoPRO, CADSTAR, PADS, P-CAD, Protel, SCICARDS, and EDIF. The standard price is $479. The software is compatible with the company's pc-board-design tools, which start at $1079. **MicroSim Corp**, Irvine, CA. (714) 770-3022. **Circle No. 352**

Deep-submicron delay-calculation tools offer accurate timing results. The Fasnet RC Extractor and Fasnet Delay Calculator provide prelayout and postlayout delay prediction of deep-submicron designs. According to the company, the tools provide delay calculations within 2 to 4% of Spice calculations. The two products together cost $20,000 for a fixed-node license and $26,000 for a floating license. **High Level Design Systems**, Santa Clara, CA. (408) 748-3456. **Circle No. 353**



FPGA and complex-PLD-design tools accommodate a variety of design methods. FPGA Designer and PLD Designer integrate with the company's line of design-entry, synthesis, and board-level verification software. The tools let you mix top-down and bottom-up design within a single environment. According to the company, the tools have been documented in PREP benchmarks to produce results within 15% of hand-crafted, schematic-based field-programmable gate-array (FPGA) designs. The tools are available for Unix workstations and cost $15,000 each; a combined package (PIC Designer) costs $23,000. Language synthesizers for Verilog HDL and VHDL are available separately for $12,000. **Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234. **Circle No. 354**

Place-and-route system combines channel- and area-based technologies. The SVR SonIC system uses the area-based technology from the company's GARDS product and the channel-based technology from the company's SC product. According to the company, the tool offers layout densities of an area-based place-and-route system with the turnaround time of a channel-based place-and-route system. The company plans to release the software in the second quarter with a price from $250,000 to $960,000, depending on the configuration. **Silicon Valley Research**, Mountain View, CA. (415) 962-3000. **Circle No. 355**

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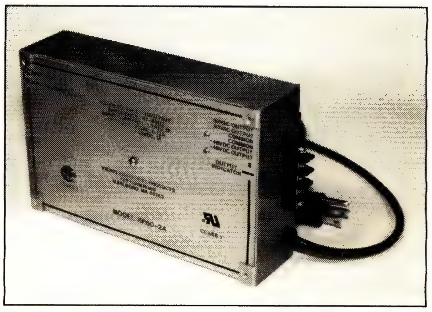
Dual-output chassis-mount power supply for harsh environments. The CM2.15.50 provides ±15V at ±50 mA. Specifications include a voltage accuracy of ±0.5%; line and load regulation of ±0.04%; and 1-mV-rms noise and ripple. Short-circuit protection is provided with foldback current limiting. The case measures 4×2.7×1.4 in. and has an operating temperature of –25 to +50°C. Input options are 100, 115, 220, 230, and 240V ac. $64.83 (100). **Calex Manufacturing Co Inc**, Concord, CA. (510) 687-4411. **Circle No. 359**

Modular, open-frame power amplifier provides one to four channels. The PS24 power amplifier drives 4 and 8Ω loudspeakers in custom sound systems, precision servo motors, and other devices. The unit provides 100W-rms power or 200W pk power with voltage and current limits of ±40V and 10A, respectively. Maximum harmonic distortion is 0.01% at 1 kHz. A one-channel unit costs $199, and a four-channel unit costs $259. **Marchand Electronics Inc**, Webster, NY. (716) 872-0980. **Circle No. 360**

30W external switcher accepts 85 to 264V ac. The PUP30 Series of desktop power supplies is available in single-, dual-, and triple-output versions. The polycarbonate case measures 5.79×2.95×1.65 in. An IEC320 input connector allows worldwide use with any power cord. Output is through a five-pin DIN connector. Line regulation is a ±0.5%, and output ripple is <1% peak. The unit provides protection against overvoltage, short-circuit, and input-surge conditions. The series is UL1950-recognized and CSA 22.2- and TUV-certified (per EN60950). Each unit also has an integral EMI-filter-limiting conducted emissions to VDE Level B and FCC Class B. $30 in OEM quantities. **International Power Sources Inc**, Ashland, MA. (508) 881-7434. **Circle No. 361**

Efficient 60W dc/dc converter needs no heat sink. The 2.94×2.41×0.43-in. dc/dc converter has 86% efficiency for the 5V version and 82% efficiency for a 3.3V (45W) version at full output power. Case temperature increase above ambient at full power is typically 30°C with 1 m/sec airflow. Thermal protection activates if case temperature reaches 115°C. The converters have 1500V input-to-output isolation, an adjustable output voltage, remote on/off control, overvoltage protection, and a low-input shutdown function that protects from harmful discharging of batteries during mains failure. $61 (500). **Ericsson Components AB**, Kista, Sweden. +46-8-721 6935. **Circle No. 362**



Ringer power supply accommodates 54 phones and costs $164 (1000). The RP60 ringer power supply is UL-recognized and CSA-certified. The unit comes in an 8×5.09×2.12-in. case and provides 93V ac biased at –48 or –24V dc. Input voltage range is 180 to 264V ac. **Viking Industrial Products**, Marlborough, MA. (508) 481-4600. **Circle No. 363**

6W, high-reliability dc/dc converters in a 0.35-in.^{3} package. The DHC2800 series converters have an input-voltage range of 11 to 50V and are available with single outputs of 3, 5, 12, or 15V. The dual-output versions with 5W power output are available in ±12 and ±15V versions. The converters operate from –55 to +125°C and feature

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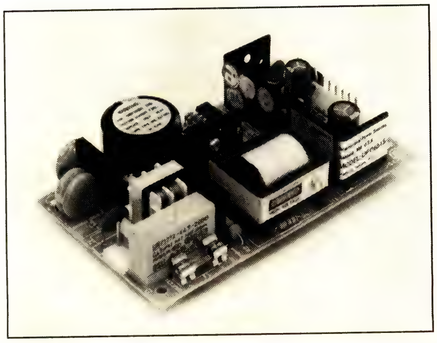
short-circuit protection, remote output-voltage sensing, 500V isolation, and up to 78% efficiency. Singles cost $225 (100), and duals cost $240 (100). **Apex Microtechnology Corp**, Tucson, AZ. (602) 690-8600. **Circle No. 364**

Triple-output, 20W dc/dc converters have four-to-one input range and power-sharing capability. The TWR Series dc/dc converters have a primary 5V output that can source up to 3A, and the auxiliary ±12 or ±15V outputs can provide up to ±500 mA. The converters accept any combination of currents, provided that total module power output does not exceed 20W. The D-12 model has a 9 to 36V input range, and the D48 model has an 18 to 72V input range. Line and load regulation are ±1 and ±2%, respectively, for the 5V output and ±5% for the secondary outputs. The converters have nonlatching output-current limiting, input overvoltage protection, input reverse-polarity protection, and output overvoltage clamping. The devices come in a 2×2×0.45-in. package and cost $74 (100). **Datel Inc**, Mansfield, MA. (508) 339-3000. **Circle No. 365**



65W ac/dc power supply costs $40 in OEM quantities. The UP065 ac/dc switching power supply comes in an open-pc-board format measuring 3×5×1.2 in. It operates from a 90 to 264V-ac input and is available in single- and triple-output models. The supply features output-overload and short-circuit protection, efficiency of 75%, holdup time of 16 msec, and I/O isolation of 3750V ac. The supply is UL 1950-recognized, and certified under CSA 22.2, no. 234, no. 950, and TUV per EN60950. Each unit has an EMI filter, limiting conducted emissions to VDE/FCC class B levels. $69 (one). **International Power Sources Inc**, Ashland, MA. (508) 881-7434. **Circle No. 366**

DC/DC converters provide up to 1000W at 82% typ efficiency. The MD series of dc/dc converters comes with one to nine fully regulated outputs from 2 to 48V. Features include current-limiting protection, current sharing with N+1 redundancy, overvoltage and overtemperature protection, low-voltage cutoff, and fully isolated outputs. Operating temperature range is 0 to 50°C. 600W models cost $595 (50). **Omega Power Systems Inc**, Chatsworth, CA. (818) 727-2216. **Circle No. 367**

10W switching power supply provides 100 to 1000V. The SL Series of high-voltage power supplies provides a single fixed-dc output from a 24V input. The supply measures 3.75×1.5×1 in. and has ripple and load regu-

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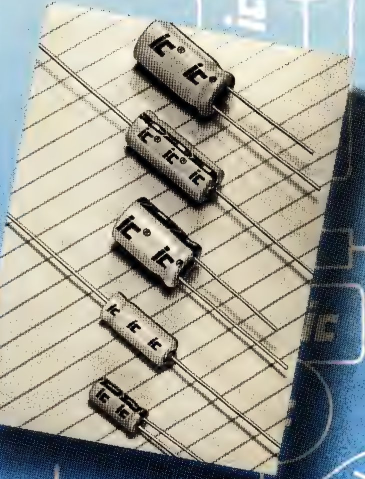

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lation of ±1%. $149 in small quantities. **EMCO High Voltage Supply Co**, Sutter Creek, CA. (209) 223-3626.
Circle No. 368

DC/DC converters provide 500 and 1000V outputs at 1.25W. The AV series of high-reliability, high-voltage converters has input ranges of 5, 12, 24, and 28. The 500V converters measure 0.5×0.5×0.4 in., and the 1000V converters measure 0.5×0.5×0.5 in. Operating temperatures range from –25 to +70°C without a heat sink or derating. An operating-temperature range of –55 to +85°C is available. The converters cost $80.12. **Pico Electronics Inc**, Mount Vernon, NY. (914) 699-5514.
Circle No. 369

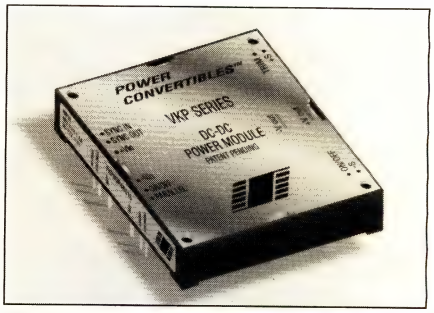
DC/DC converters have internal Pi filter to reduce reflected ripple current. The A series dc/dc converters for telcommunications applications have input-voltage ranges of 9 to 18, 18 to 36, or 36 to 72V. The converters offer single or dual outputs with voltages of +5, 12, +15, –5, –12, and –15V. Maximum power output is 10W, and maximum conversion efficiency is 85%. The converter comes in a 1×2×0.4-in. package. $30 (OEM). **Semiconductor Circuits Inc**, Windham, NH. (603) 893-2330. **Circle No. 370**

30W dc/dc converters suit 3.3V logic. The NL Series of dc/dc converters accepts an input-voltage range of 4.75 to 7V dc. Output voltage trim is adjustable. The series offers 25W output-power that can be trimmed to 30W. The converters are available in 2×2×0.5- and 1×2×0.5-in. packages. From $38 (OEM). **Semiconductor Circuits Inc**, Windham, NH. (603) 893-2330. **Circle No. 371**

Adapter permits upgrading from 5V processors to 3.3V 68040V and 68060 devices. The Correct-A-Chip adapters provide all the circuitry to convert the standard 5V power supply to the 3.3V that the new processors require. Adapters for 3.6V operation are also available. $195 (100). **Aries Electronics Inc**, Frenchtown, NJ. (908) 996-6841. **Circle No. 372**

Radiation-hardened, 20W dc/dc converters have an internal filter that meets MIL-STD-4161C. The MDI Model 3107R operates from a 16 to 50V input and is available in single-, dual-, and triple-output versions. Typical output performance includes a dc output ripple of 50 mV p-p and efficiency ratings to 85%. The converter weighs 50g and comes in a 2.12×1.12×0.495-in. package. From $915 (10). Also available are the 3108R, which operates from a 120V-dc input, and the 3109R, which operates from a 270V-dc input. Prices for both start at $985 (10). **Modular Devices Inc**, Shirley, NY. (516) 345-3100.
Circle No. 373

100W dc/dc converter module measures 2.28×2.4×0.5 in. The VI-J00 converters are available with input ranges of 10 to 400V and output voltages of 1 to 95V. The converters feature approval by BABT, UL, CSA, TUV (IEC 950), and BSI. Typical E-grade VI-J00 units cost $100. **Vicor Corp**, Andover, MA. (508) 470-2900. **Circle No. 374**



60W dc/dc converters offer high efficiency. The VKP60R offers typical efficiencies ranging from 84% for 3.3V output to 91% for 15V output. The converter comes in a 2.3×2.4×0.45-in. package and operates from 36 to 72V. Load and line regulation are ±0.05% max. The units offer output-overvoltage, overcurrent, and overtemperature protection. Full power is available up to a base-plate temperature of 100°C. $93 (500). **Power Convertibles Corp**, Tucson, AZ. (602) 628-8292.
Circle No. 375

2.4×4.6-in. dc/dc-converter module has single, dual, and triple outputs to 150W. HD series dc/dc converters accept input voltages of 18 to 36, 20 to 60, or 36 to 72V and have regulated single outputs of 5, 12, 15, 24, and 48V. Dual-output versions offer ±5, ±12, ±15, and ±24V; triples offer 5 and ±12 or 5 and ±15V. The supplies feature active current sharing, continuous

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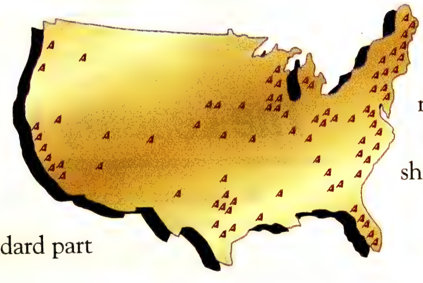

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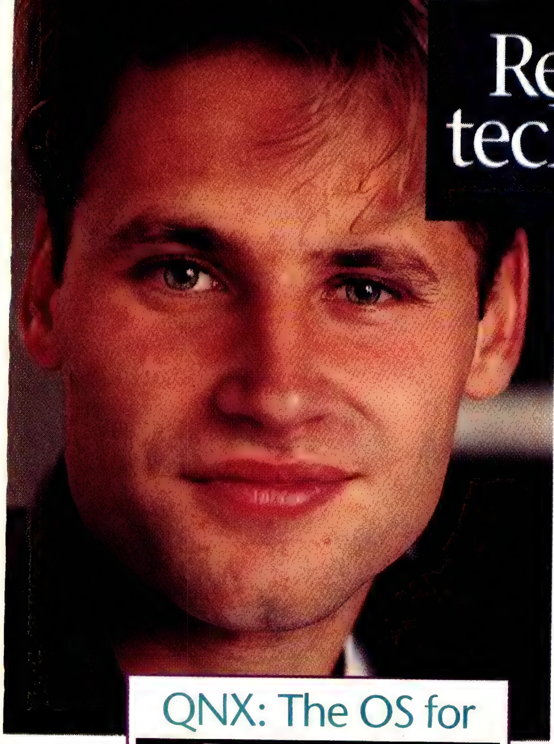

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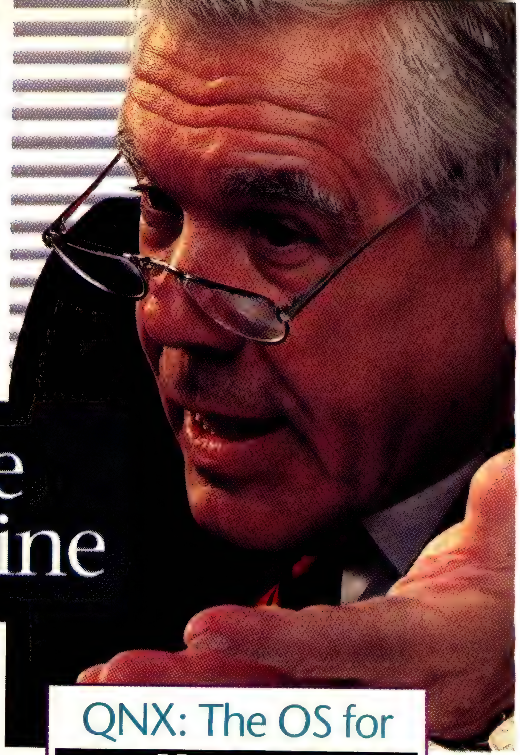

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short-circuit protection, 500V-dc isolation, a fixed switching frequency of 250 kHz, and a typical efficiency of 80%. OEM quantity price is $122.20 for singles, $137.35 for duals, and $146.95 for triples. **Wall Industries**, Exeter, NH. (603) 778-2300.

Circle No. 376

5W dc/dc converters in a 1×1×0.45-in. package fit industry-standard pinout. The XWR Series of dc/dc converters fits the industry-standard pinout for 3 to 10W converters, even though their case is much smaller than the standard. The converters are available in unipolar voltages of 5, 12, and 15V and bipolar voltages of ±5, ±12, and ±15V. Input ranges are 9 to 36 and 18 to 72V. Line and load regulation is ±2%, and typical efficiency is 80%. Isolation is 1200V dc min. $47 (100). **Datel Inc**, Mansfield, MA. (508) 339-3000.

Circle No. 377

110W external switching power supply accepts 85 to 264V ac. The PUP110 series of external switching power supplies is available in single- to quad-output versions. Features include an EMI filter, a 94V-rated polycarbonate enclosure, an IEC 320 input connector for worldwide use, and a five-pin DIN output connector. The unit protects against overvoltage, short circuits, and input surges. Line regulation is ±0.5%, and total output error is 3 to 5%, depending on the output. Ripple is 1% pk, and efficiency is 65% at full load. The series is UL1950-listed and CSA22.2 No. 234- and TUV (per EN 60950)-certified. MTBF is >100,000 hours. $85 (OEM). **International Power Sources Inc**, Ashland, MA. (508) 881-7434.

Circle No. 378

DC/DC converter provides 3.3V at 8A from a 5V input. The PT6501 comes in a 14-pin SIP measuring 0.36×1.64×1.16 in. It operates at 550 kHz with up to 90% efficiency. The converter is available with top, side, or no heat tabs. Features include internal short-circuit and over-temperature protection, adjustable output voltage, and a standby function. $25 (1000). **Power Trends Inc**, Batavia, IL. (708) 406-0900.

Circle No. 379

Regulated dc/dc converters have 1500V-rms isolation. The TWACB series of 3W converters comes with input-voltage ranges of 4.5 to 6, 9 to 18, and 36 to 72V. Outputs are 5, 12, 15, ±5, ±12, and ±15V. An internal Pi filter minimizes reflected ripple at the input, eliminating the need for external filtering. Line and load regulation are ±1%. $17 in OEM qty. **Polytron Devices Inc**, Paterson, NJ. (201) 345-5885.

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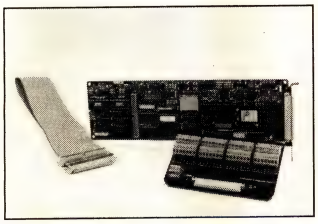
33-MHz PCI bus exerciser emulates bus traffic of absent PCI devices. The HP E2910A PCI bus exerciser lets you bring up, debug, and validate PCI designs. The bus exerciser simulates devices deterministically with bus traffic that emulates the real-world traffic conditions of a final application. The designs, which may include ICs, system motherboards, and plug-in cards, appear as emulated hardware, prototype devices, or final devices. Because you no longer have to wait for actual PCI hardware, testing can begin earlier. You can exercise all variations and test stressful corner cases within the PCI protocol using the bus exerciser. $44,900. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 8917. **Circle No. 397**

Software simplifies analysis, archiving, and printing of electrical waveforms. FlukeView provides users of the company's ScopeMeter test tool or the ScopeMeter Series II handheld test tools a customized interface for managing measurements and data on a PC. Versions are available for DOS and Windows. The ScopeMeter communicates with PCs using its optical RS-232C port. $195. **Fluke Corp**, Everett, WA. (206) 347-6100. **Circle No. 398**

Data-acquisition software operates on Macs. WorkBenchMac version 4.0 data-acquisition software for the company's data-acquisition boards includes a serial icon to support input and output from serial devices, X-Y charting, a switch icon for operator on/off manipulation, a slider icon for operator analog manipulation, an analog-meter icon for display, a menu icon to invoke menu and finder commands, an Apple-events icon to transfer data between the tool and other programs in real time, and a background-picture feature to display application processes using standard PICT format graphics files. $995. **Strawberry Tree Inc**, Sunnyvale, CA. (408) 736-8800. **Circle No. 399**

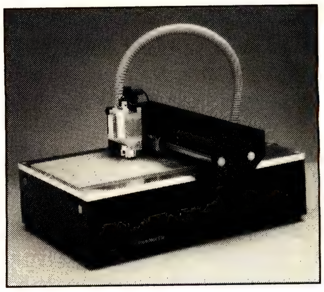


Multisensor interface card for PCs accepts 16 channels without external signal conditioning. The Model MS160x Series multisensor interface card accepts inputs from thermocouples, resistance-temperature detectors, potentiometers, resistors, strain gauges, linear-velocity displacement transformers, variable-reluctance pressure transducers, and low-level dc. The card provides 11 levels of programmable gain and 14-bit A/D resolution. Conversion rates range from 5000 to 20,000 channels/sec. Coprocessing can perform averaging and other computations on the data to reduce PC overhead. Prices include the card, an analog terminal block, control software, the LabTech Notebook driver, and a 5-ft-long cable. From $1795. **Industrial Computer Source**, San Diego, CA. (800) 523-2320. **Circle No. 400**

Differential integrated silicon pressure sensors offer ranges up to 150 psi. The MPX5500D, MPX5700D, and MPX-5999D micromachined pressure sensors have signal conditioning, temperature compensation, and calibration on chip. Pressure ranges are 0 to 75, 0 to 100, and 0 to 150 psi. Output voltages are 0.2 to 4.7V. $10 (OEM qty). **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 244-4556. **Circle No. 401**

Board-test system with 896 hybrid, bidirectional, digital channels costs $140,000. The price for the GR2280/GR2281 includes test software, three programmable user power supplies, and an analog functional-test module. You can configure the system for applications requiring lower pin counts. Prices start at <$100,000. **GenRad Inc**, Concord, MA. (508) 287-7000. **Circle No. 402**

Runtime system for PC-based data-acquisition software costs one-fourth the full-package price. The runtime system for Visual Designer costs $250 and lets you run any number of applications that you created using the full Visual Designer development system ($995). The Windows-based application generator lets you develop custom programs by drawing block diagrams of the application instead of programming in a language. **Intelligent Instrumentation Inc**, Tucson, AZ. (602) 573-0887. **Circle No. 403**



Prototype circuit-board-fabrication systems suit high-frequency applications. The 91S, 92S, and 93S Protomat circuit-board plotters provide the stability and accuracy to route two traces through a standard 0.1-in. IC grid. The systems work with dielectric materials, such as Teflon, Duroid, and polyamide, common in high-frequency work. The systems include software and hardware to take CAD-generated Gerber or HPGL-format files and create milled and drilled circuit boards that match production pc boards. The systems require no chemicals. Prices range from $8500 to $19,950. **LPKF CAD/CAM Inc**, Portland, OR. (503) 297-2720. **Circle No. 404**

High-speed development and computation software for MatLab and DSP users. The Paramex software interfaces MatLab directly to one or more TMS320C40 processors using Parallel C from 3L Ltd. The vendor claims the system accelerates signal-processing functions. A bundled MatStart package includes Paramex, a four-slot TIM-40 motherboard, a TIM-40 processing module, and the 3L single-processor C compiler for $5995. **Advanced Computing Solutions**, Beaverton, OR. (503) 626-3896. **Circle No. 405**

Data-acquisition card for PCs captures 12-bit analog signals at 100 kHz for $279. The Model 100 data-acquisition card accepts eight single-ended or four differential analog-input channels and provides four 8-bit analog output channels, 24 digital I/O lines, and three 16-bit timer/counters. Inputs are software-programmable for 0 to 5 or ±2.5V ranges. Optional software ($79) provides up to 10 simultaneous real-time instrument displays, including oscilloscope, strip chart, bar graph, X-Y plotter, and large-panel-meter readout. **Prairie Digital Inc**, Prairie du Sac, WI. (608) 643-8599.

Circle No. 406

Windows-based data-acquisition, control, and real-time analysis software accommodates >100 data-acquisition devices. DasyLab version 2 provides greater support for hardware-specific features on data-acquisition devices than did the previous version. Fast disk-streaming transfers data at >200 kHz to disk. The software can simultaneously display portions of the data, providing a visual check of the measurements. The software also has new virtual-instrument displays and improved ability to respond to events with predefined actions. $995. **Dasytec**, Amherst, NH. (603) 672-7061.

Circle No. 407

Plotting software finds best-fitting equation from 3456 linear and nonlinear equations. TableCurve 2D for Windows, version 3 is up to three times faster than previous versions, according to the vendor. The software also provides numeric, statistical, and precision summaries. To determine the best-fitting equation, the tool ranks equations based on criteria you select. You can scroll through the equations and view the corresponding curve-fit graph. The software also has improved data import, advanced analysis of curve-fit results, and tool and status bars. $495. **Jandel Scientific Software**, San Rafael, CA. (415) 453-6700.

Circle No. 408

Multimeter measures ac/dc voltage and current without a battery. Power for the heavy-duty No-Bat multimeter comes from a capacitor charged by applying the test leads to an ac or dc source. The meter operates for more than 2 hours after a 3-minute charge. The 5.7×2.7×1.5-in. multimeter weighs 12 oz. It measures 2 to 750V ac, 200 to 1000 mV dc, ac or dc current from 2 mA to 10A, and resistance from 200Ω to 20 MΩ. $79. **Extech Instruments Corp**, Waltham, MA. (617) 890-7440. **Circle No. 409**

Software speeds development and testing of peripherals. The Peripheral Test and Development System (TDS) provides an interactive programming environment for full control of the test environment. The TDS is available for PC/AT attachment-packet-interface CD-ROM ($4795), enhanced IDE ($4495), SCSI ($6995), and PCMCIA ($7995) interfaces. The software runs under Windows. **Zadian Technologies Inc**, San Jose, CA. (408) 894-0800.

Circle No. 410

EISA-bus extender lets you add and remove boards without powering down the system. The EISAIX32 uses MOSFET drivers and analog switches to isolate power and signal lines to the board under test. The extender also provides header pins for connecting a logic analyzer. The 4.6-in.-high extender costs $395. The company also offers the 1.3-in.-high EISASX4 wear-out extender for heavy use. The $69 device prolongs the life of the extender connector. **Adex Electronics**, Lake Forest, CA. (714) 768-3211.

Circle No. 411

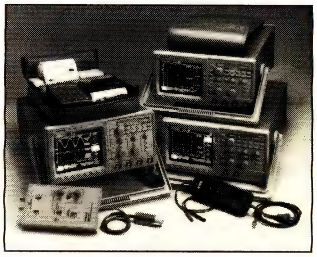
Mathematical-analysis software runs under Windows and on Macintosh systems. The Theorist 2 mathematical program combines the solution of algebraic equations with 2- and 3-D graphing. A graphical user interface using standard math notation avoids the need for a specialized programming language. $299. **Waterloo Maple Software**, Waterloo, ON, Canada. (519) 747-2373.

Circle No. 412

Calibration system functionally tests and calibrates electrical test equipment. The Model 9100 universal calibration system works with handheld and benchtop DMMs, analog multimeters, clamp meters, power harmonic analyzers, electronic thermometers, panel meters, chart recorders, and data loggers. Options extend the system to cover analog and digital oscilloscopes with bandwidths to 250 MHz and counter/timers. An advanced procedure mode guides an untrained operator through the calibration process, allowing the operator to test and calibrate a typical instrument in <5 minutes. The basic system costs $9995. **Wavetek Corp**, San Diego, CA. (619) 279-2200.

Circle No. 413

Device tests of ac and dc power supplies and dc/dc converters. The 3600 automatic power-supply tester tests all functions standalone or under computer control. The unit includes a 600-VA ac source, four electronic loads, four peak-to-peak detectors, a controller, and built-in Centronics and RS-232X interfaces. The standard system tests power supplies to 500W, and options allow testing above 500W. $10,882. **IMC-Prodigit**, San Jose, CA. (408) 441-9614. **Circle No. 414**



DSO family provides bandwidths to 400 MHz. The TDS 400A series digital storage oscilloscopes (DSOs) sample at up to 100M samples/sec and provide up to 12-bit resolution in a high-resolution mode. Standard record length is 30k samples, which you can optionally increase to *120k samples*. The two-channel, 200-MHz TDS410A costs $4950, the four-channel, 200-MHz TDS420A costs $6295, and the four-channel, 400-MHz TDS460A costs $7685. Options include a differential amplifier providing 10-μV sensitivity, a 3.5-in. floppy-disk drive, a printer pack,

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an FFT/math option for harmonic analysis of signals in the frequency domain, a high-voltage probe, and an RS-232C/Centronics interface. **Tektronix Inc**, Beaverton, OR. (800) 426-2200. **Circle No. 415**

AC power source and analysis instruments suit compliance testing. The 8000 Series ac power-source and analyzer systems suit power-supply and uninterruptible-power-supply testing, automatic-test-equipment applications, power-factor-correction-equipment evaluation, and compliance testing to regulatory standards. The systems perform harmonic synthesis and analysis; simulate power-line disturbances including surge, sag, drop, step, sweep, and delay; and have a Windows-based graphical user interface. The systems range from the Model 8141 ($14,575) with 1.4-kVA capacity for single-phase applications to the Model 8333 ($23,175) with 3.3-kVA capacity for three-phase applications. **Pragmatic Instruments Inc**, San Diego, CA. (619) 271-6770. **Circle No. 416**

Two-channel DSO board for Macintosh NuBus samples at 100M samples/sec. The MacQuire plug-in data-acquisition, digital-storage-oscilloscope (DSO) board comes with LabView graphical instrumentation software. The board offers a 130-MHz bandwidth and a 1-Mbyte memory, expandable to 4 Mbytes. The board has an equivalent-sampling rate of 12G samples/sec for repetitive signals. It provides software-selectable triggering with adjustable coupling, slope, and level settings. Dead time from the end of one sweep to acceptance of the next trigger is <400 nsec. $4800. **Information Systems Technology Inc**, Hinsdale, IL. (708) 887-1911. **Circle No. 417**

Low-cost RF-network analyzers cover 300-kHz to 3-GHz frequency range. Four RF-network analyzers provide automated measurement for manufacturers who tune and test RF devices in cable, wireless-communications, and consumer-electronic products. The 8711B ($9500) and the 8712B ($16,500) perform scalar and vector measurements, respectively, over a frequency range of 300 kHz to 1.3 GHz. The 8713B ($14,500) and the 8714B ($21,500) perform scalar and vector measurements, respectively, over the 300-kHz to 3-GHz frequency range. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9018. **Circle No. 418**

Scope software simplifies moving waveforms and measurements to Windows applications. Waveform Manager Lite ($99) and Waveform Manager Pro ($199) work with the Fluke ScopeMeter, Tektronix TekMeter, and the Tektronix 22x and 222A oscilloscopes. Both versions let you transfer setups and waveforms, annotate waveforms, scale images, and use the Windows clipboard to copy image into applications. The Pro version also adds waveform-measurement features, including cursors, parameter measurements, and harmonic analysis. **Metratek**, Hillsboro, OR. (503) 640-4906. **Circle No. 419**

Software links data acquisition with publication-quality graphics in real time. SigmaLab Link links the company's Notebook or other data-acquisition software and Jandel Scientific's SigmaPlot or SigmaStat. Real-time transfer of data between the two applications lets you immediately view high-quality graphics presentations. The tool costs $49.95. **Laboratory Technology Corp**, Wilmington, MA. (508) 657-5400. **Circle No. 420**

PCMCIA card converts analog inputs at up to 100k samples/sec with 12-bit resolution. The DAQP-12 Type II PCMCIA card accepts eight differential or 16 single-ended analog inputs and is expandable to 256 inputs. The input ranges are programmable from ±10 mV to ±5V. A 512-sample data FIFO buffer enables full-speed data acquisition under various operating systems, including DOS and Windows. The card converts at full speed while using random channel ordering and gain selection on up to 256 channels. An internal clock and divider provide accurate sampling rates from 0.01 Hz to 100 kHz. The card also provides four digital-input and four digital-output channels. The card costs $695, including software drivers and a dynamic-link library for various programming languages. **Quatech Inc**, Akron, OH. (216) 434-3154. **Circle No. 421**

Fortran 77 compiler for Power Macintosh offers fast execution. The LS Fortran compiler for the Power Macintosh is source-code-compatible with the company's LS Fortran 3.3 version. According to the company, the DLinpack benchmark runs at 13.5 MFLOPS, providing a 625% increase in execution speed over the previous version. The compiler costs $695 and includes versions for both PowerPC- and 68000-based Macintoshes. **Language Systems Corp**, Sterling, VA. (703) 478-0181. **Circle No. 422**

Pressure transducers use digital compensation. The Models 9400 and 9401 pressure transducers are available in pressure ranges from 0 to 5 to 0 to 750 psi, gauge or absolute. Digital algorithmic-compensation circuitry corrects zero, span, and linearity errors over the operating pressure and temperature range of the transducer. Static accuracy is ±0.1% full scale, and thermal stability is ±0.001%/°C. A media-isolated, silicon, piezoresistive sensor allows the transducers to work with all media, including corrosive fluids and gases. $400. **Pressure Systems Inc**, Hampton, VA. (800) 678-7226. **Circle No. 423**

Low-cost EPROM and EEPROM programmers connect to parallel printer port. The Rommaster/1, a 32-pin, single-socket programmer, costs $199, including an ac adapter, cable, and software. The programmer supports 24-, 28-, and 32-pin EPROMS, EEPROMs, flash EPROMs, serial EPROMS, GAL 16V8, and GAL 22V10. Adapters let you program 87xx and PSD 3xx microcontrollers. A 32-pin,

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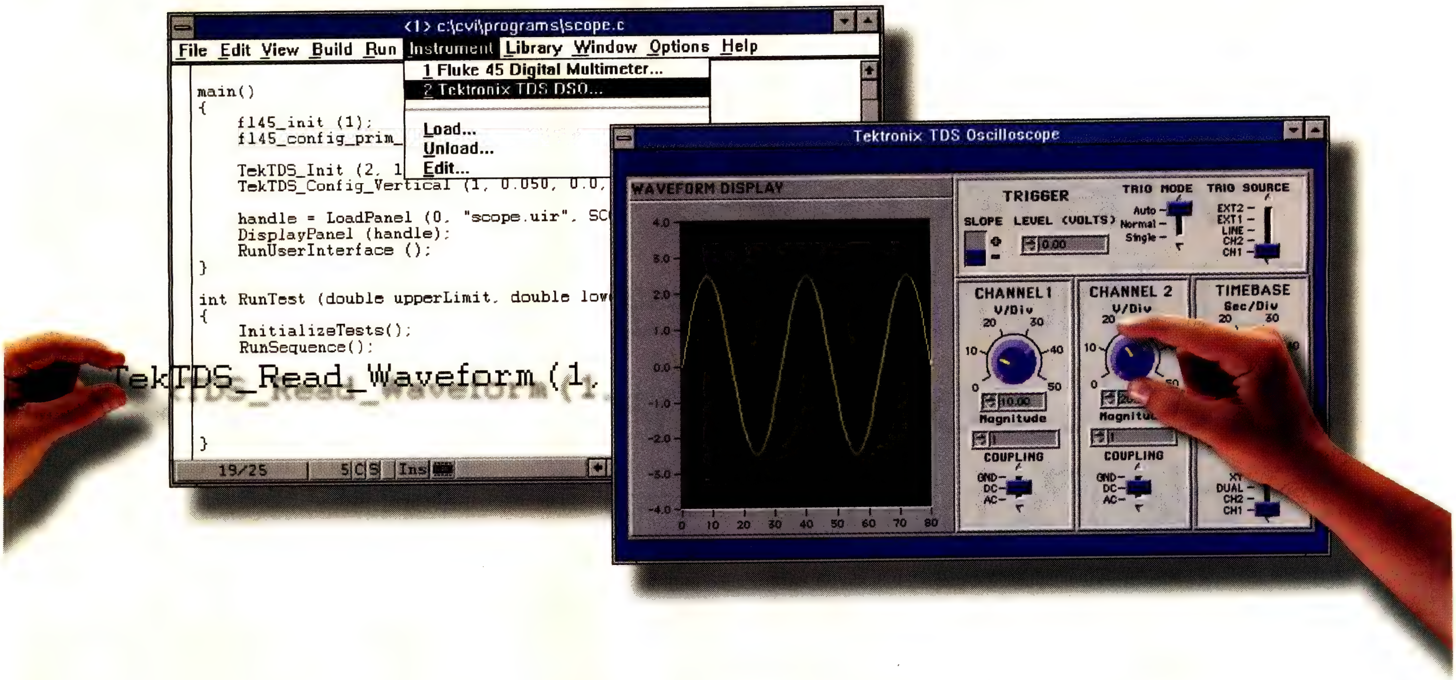

```
main()
{
    f145_init (1);
    f145_config_prim_

    TekTDS_Init (2, 1
    TekTDS_Config_Vertical (1, 0.050, 0.0,

    handle = LoadPanel (0, "scope.uir", SC
    DisplayPanel (handle);
    RunUserInterface ();
}

int RunTest (double upperLimit, double low
{
    InitializeTests();
    RunSequence();
TekTDS_Read_Waveform (1,


}
```

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four-socket gang programmer costs $279. **Xeltek**, Sunnyvale, CA. (408) 524-1932. **Circle No. 424**

Two-line telephone line simulator is portable. The TLS-3A telephone-line simulator simulates a two-line central-office or private-branch exchange (PBX). The product tests and demonstrates two analog telecommunications devices, such as phones, fax machines, and modems. It also tests PBX- and key-system installations before connecting central-office lines. Key features include precise call-progress tones for dial, busy, reorder, and ring-back; typical central-office battery feed; ac ringing voltage; two loop-start lines with single-talk path; and ac powering. New features for this version include dial-up test tones, forced disconnect pulse, and secondary dial tone. $375. **Teltone Corp**, Bothell, WA. (206) 487-1515. **Circle No. 425**

Parallel-port data-acquisition module adds analog output option. The Datashuttle module with digital and analog I/O capability has eight analog inputs with either 12- or 16-bit resolution and eight digital I/O lines. The new option adds two 12-bit analog output channels with a 2-kHz update rate. Output-voltage ranges are 0 to 10, 0 to 5, 0 to 2, ±5, ±2.5, and ±1V. Output-current ranges are 4 to 20 mA source and sink with 3 to 30V compliance. All ranges and resolutions are under software control. The 7.5×5.5×2-in. module weighs <2 lbs and connects to any PC with a parallel port. Prices start at $995. **Strawberry Tree Inc**, Sunnyvale, CA. (408) 736-8800. **Circle No. 426**

Nanovolt/micro-ohm meter has 1.3-nV-rms noise. The HP 34420A nanovolt/micro-ohm meter has $7\frac{1}{2}$-digit resolution, 2-ppm basic 24-hour dc-volt accuracy, and selectable analog and digital filters. The meter has an integral two-channel, programmable scanner for automated ratio and difference measurements. The meter also has conversion routines that display thermocouple, thermistor, and resistance-temperature-detector readings directly as temperatures with resolution to 0.001°C. Other features include scaling and statistical-math functions, storage for 1024 readings, a chart recorder analog input, and RS-232C and IEEE-488 interfaces. $3195. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9033. **Circle No. 427**

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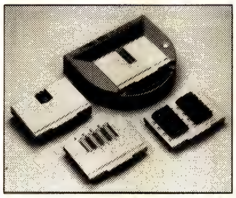

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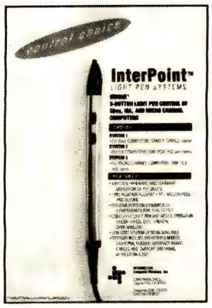

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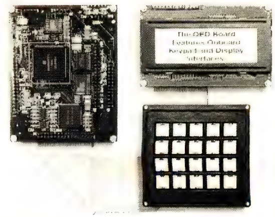

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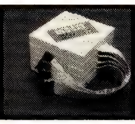

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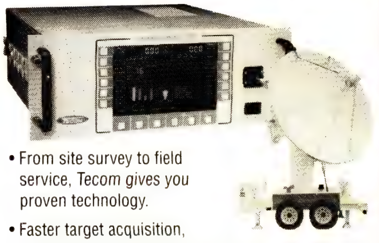

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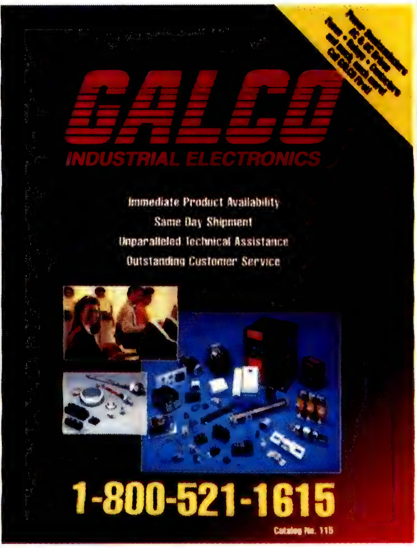
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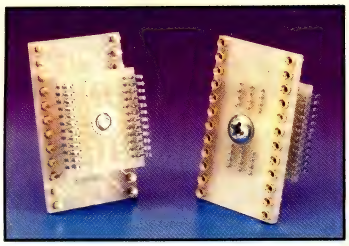

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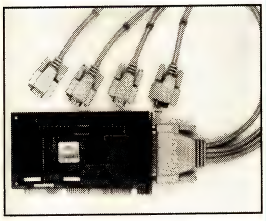

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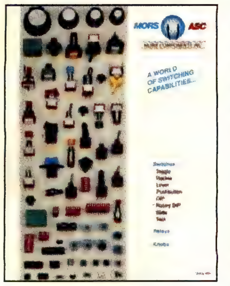

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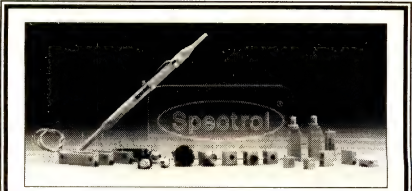

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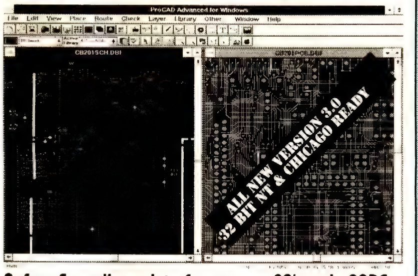
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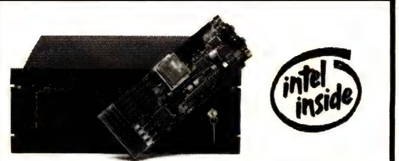

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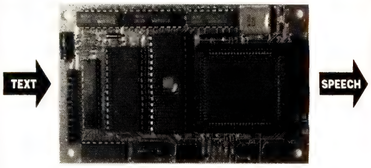

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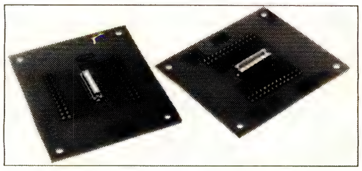

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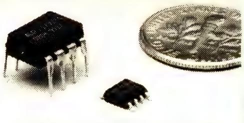

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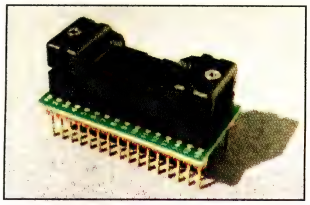

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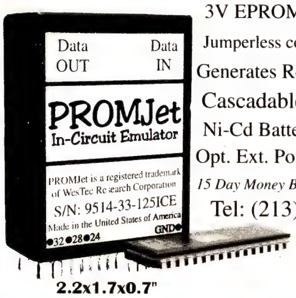
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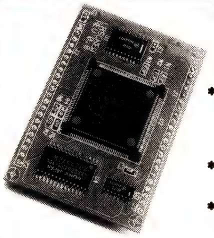

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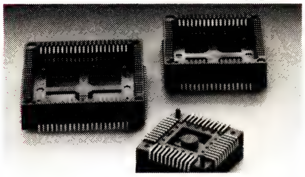

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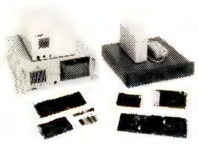

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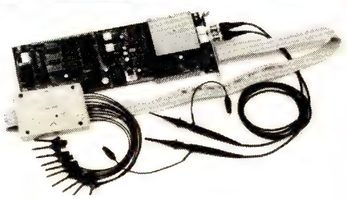

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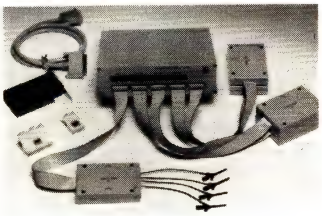

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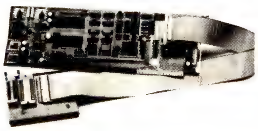

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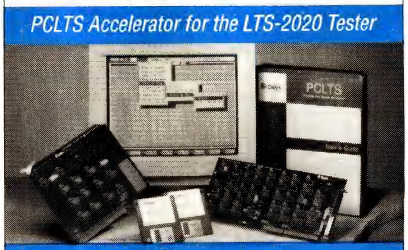

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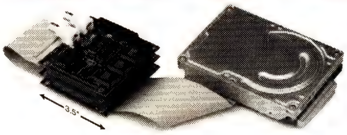

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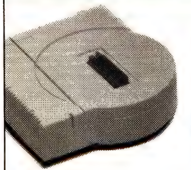

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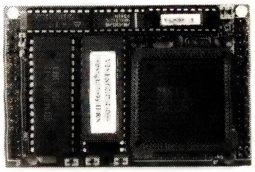

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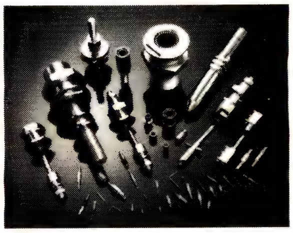

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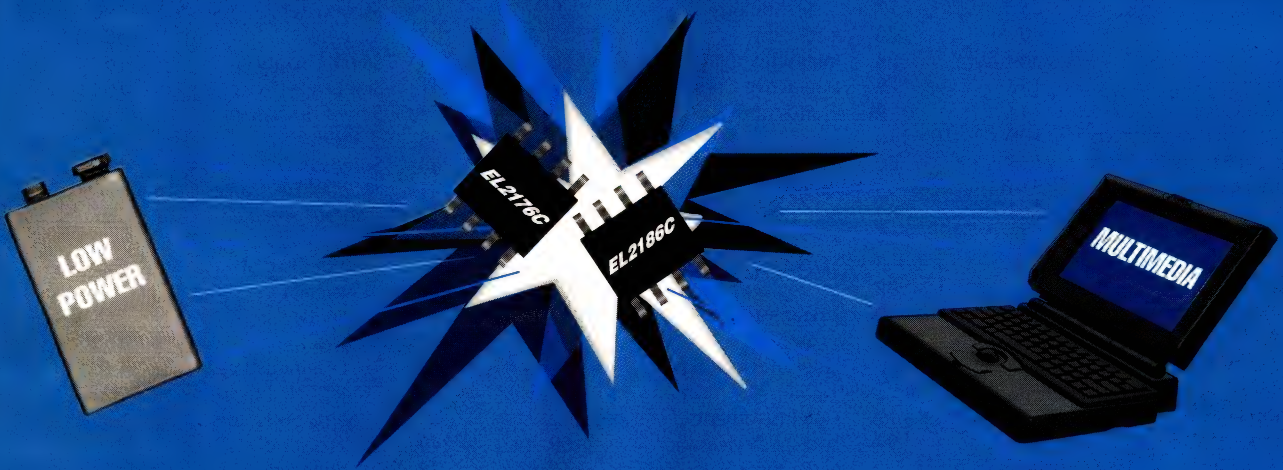

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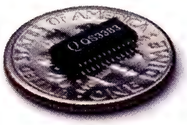

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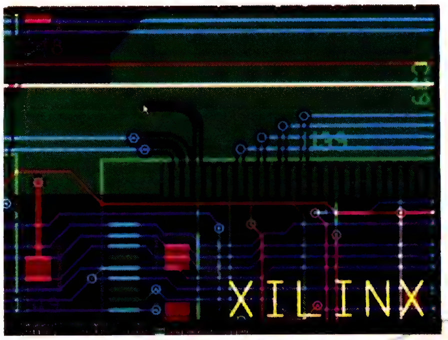

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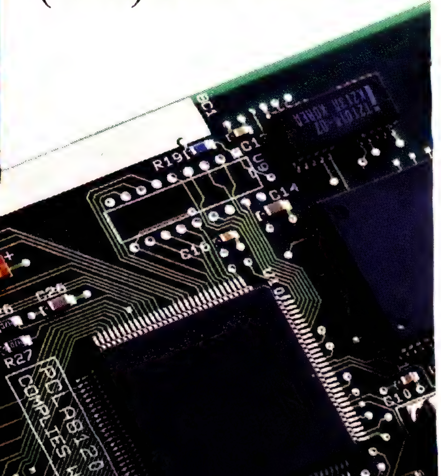

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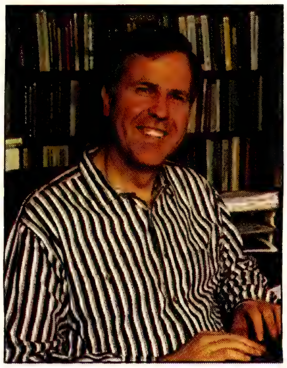

DAVID BRUBAKER,
FUZZY-LOGIC CONTRIBUTING EDITOR

Warning: Your current fuzzy systems are only half fuzzy

Ed note: The following letter is one of several the author recently received from readers.

I really enjoyed your column "Dismantling a fuzzy rule-based system shows its inner workings"** (EDN, **November 10, 1994, pg 189). Your column summarized fuzzy very well. I am one of the frustrated engineers who's really interested in fuzzy logic but hasn't yet had the chance to apply it on the job.

One concern regarding output membership functions: It seems like crisp outputs would be the same whether the output membership functions were symmetrical triangles or just singletons. If this [assumption] is true, why would we ever bother with triangles when singletons are easier to defuzzify?

Ray Johnson,
Lockheed Idaho Technologies

* * *

A kindred spirit! Ray is the only other person I know of who has realized that centroid defuzzification essentially is the same as using singletons. His letter also sparks a discussion I promised earlier on regarding defuzzification. Note that the shortcomings of fuzzy logic I point out are not weaknesses, but rather commentary on how fuzzy logic is currently being used in system design.

First, let's review what defuzzification is. Most fuzzy rule-based systems use membership functions to represent input conditions and output actions. These functions represent fuzzy sets or fuzzy values. Examples of fuzzy values include *low*, *fast*, or *heavy*. Examples of numeric (or crisp) values, with which we have had more experience, are 2, 5, or 23,462.789.

In a fuzzy system, when several rules fire simultaneously, the kernel typically defuzzifies and combines the specified output actions, expressed as fuzzy values, into a single, crisp output. (I use "typically" here because some systems do not defuzzify but rather maintain the output in its fuzzy form, often to pass on to a subsequent fuzzy stage.) Defuzzification is the operation that transforms a fuzzy value into a crisp equivalent.

Currently, you can select from a number of techniques for defuzzification. The centroid, or center-of-gravity (COG), approach is the most popular. The kernel first lops off the top of each fuzzy output value at the truth value of the fired rule and then calculates the center of mass of each participating output. The center of these centers of mass indicates the single output action.

I know of four problems associated with centroid defuzzification. The first is computational intensity. Although calculating areas is not excessively difficult for triangular and trapezoidal functions, in real-time systems running on microcontrollers, the impact of doing so may be critical.

An example will best illustrate the second problem. Say a given output range has a high-end limit of 10. A membership function ranging, say, from 8 to 10 represents the maximum fuzzy value. Its COG is in the neighborhood of 9. Because centroid defuzzification calculates system outputs from COG figures, no system output greater than the COG of this function, that is, 9, will be possible—despite the desired *maximum* being 10. Of course, we can artificially overcome this shortcoming by extending the output domain beyond its actual limit and creating the membership function at the extreme, so that its COG coincides with the desired limit. However, this deviates from the close mapping between model and real world, which is a strength of a fuzzy system.

The third problem with centroid defuzzification is the point Ray Johnson makes in his letter. If output membership functions are vertically symmetric, the only difference on the resulting output value between them and singletons are the weights associated with different function areas. This situation results because the COG of a vertically symmetric function lies on a single vertical axis. Independent of whether the rule fired strongly or weakly (which occurs in response to changing input values), the designated output value remains constant.

Function areas, which singletons do not have, and which are used for weights when combining several actions, make up the fourth centroid problem. This issue tends to

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be a bit philosophical. Consider two output functions, one wide and one narrow. That the wide one is wide means we are less certain as to its meaning, that is, "I will accept any output in this admittedly broad range." And the narrow one's being narrow implies that we are quite certain as to its meaning, that is, "I want an output that is constrained to this specific region." "Wideness" corresponds to uncertainty and imprecision; "narrowness" corresponds to certainty and precision. If two rules fire with the same truth value, with centroid defuzzification, the wide (imprecise) output will take precedence over the narrow (precise) output. To me, this is counter-intuitive.

A better scheme would weight singletons based on the "area" of the region in the input space for which the given rule is active. About three years ago, I developed an inference method using this approach and called it "weighted singleton inference." I still use it, but no one else seems to have picked it up. I attribute this, at least in part, to a concurrent study I conducted comparing centroid, standard singletons, and weighted singletons in both closed- and open-loop control. For the most part, results were indistinguishable from the technique used.

While I'm on the soapbox, I have three more observations concerning defuzzification and centroids.

Fuzzy rule-based systems of today are only half fuzzy. A system's inputs are fuzzy because of the fuzzy input values, but, when using singleton output values or fuzzy output values with centroid defuzzification, outputs are not fuzzy. Any apparent fuzziness at the output comes from overlapping fuzzy input functions.

If a "half-fuzzy" system utilizes fuzziness only at its inputs, then, to be "fully fuzzy," a system must have both fuzzy inputs and fuzzy outputs. Small changes in the inputs must result in small changes in the output(s), even when only one rule is firing. In a fully fuzzy system, one would expect to see regions of constant output value only when using a crisp output function (a singleton), in addition to the fuzzy output functions.

Most fuzzy systems use fuzziness only as a means of interpolating outputs between crisp regions of constant value. With centroid and singleton defuzzification, a fuzzy-rule-based system is nothing more than a representation of a system response function obtained by dividing the input space into crisp, noncontiguous regions, assigning a constant output value to each of these regions, and letting the "fuzziness" provide smooth transitions (an interpolation) between the constant output values. Any interpolation system would work as well or better, and, for a two-input system, would be easier to implement.

The overall response of "half-fuzzy" systems is largely insensitive to the type of defuzzification used. So long as the transitions are smooth and interpolated (that is, they don't result in values outside the constant regions being connected) fuzzy systems are actually quite tolerant of various methods of transition calculation. Singletons, centroids, and weighted singletons all result in similar response functions, although centroids tend to have more "noise" when more than two rules are firing.

So, what does this all mean? First, we need a more powerful inference method (and, therefore, defuzzification technique), one that fully utilizes fuzziness at both input and output, and one that allows us to create "fully fuzzy" systems. This move is more difficult than it may seem, but it's evolving. Until its arrival, fuzzy-rule-based-system designers would do well to discard centroid as a defuzzification technique. The results are not worth the additional complexity. Use singletons instead; or, if you're a nonconformist, use weighted singletons. If you send me a self-addressed, stamped envelope, I'll send you a paper I wrote on them.

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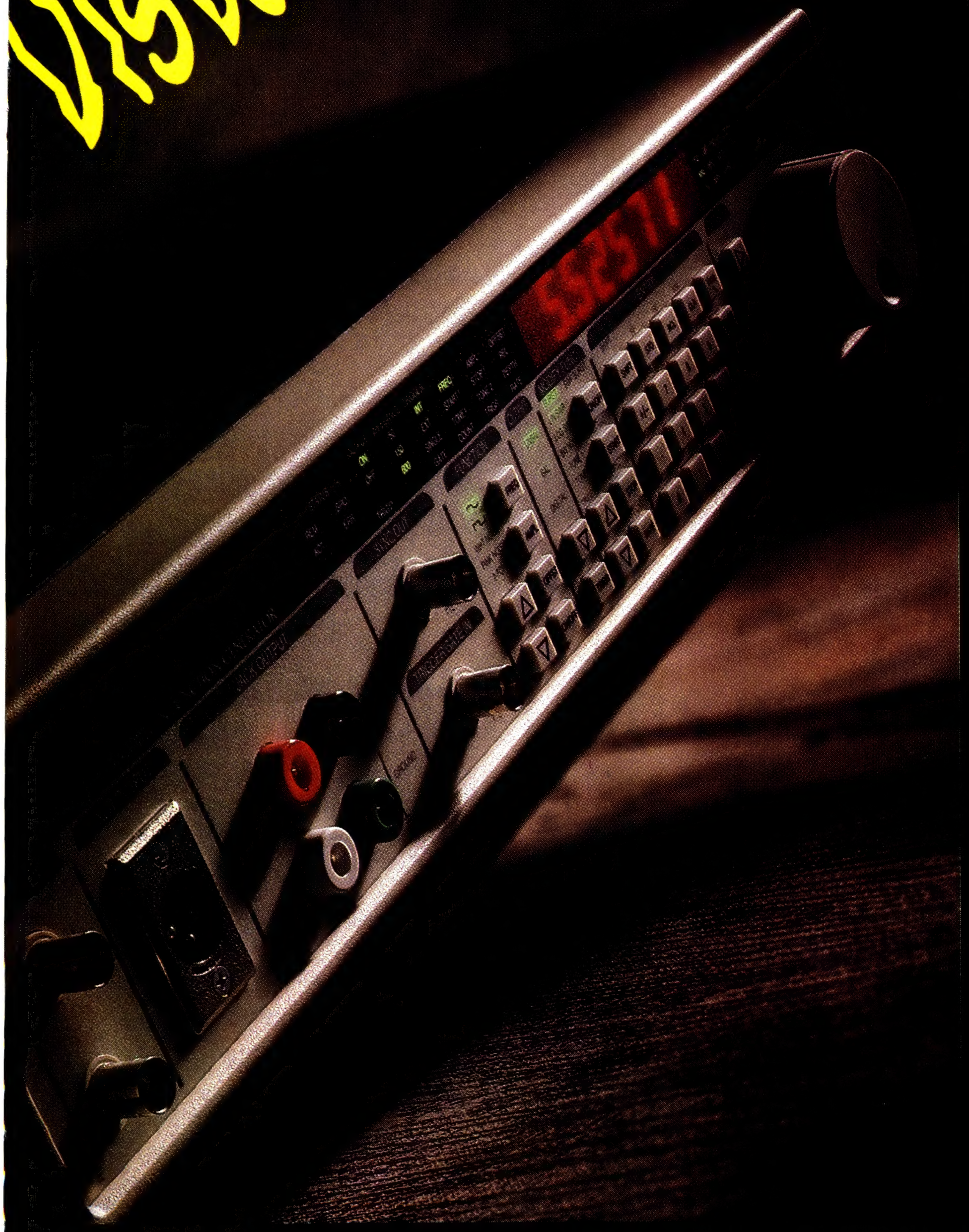

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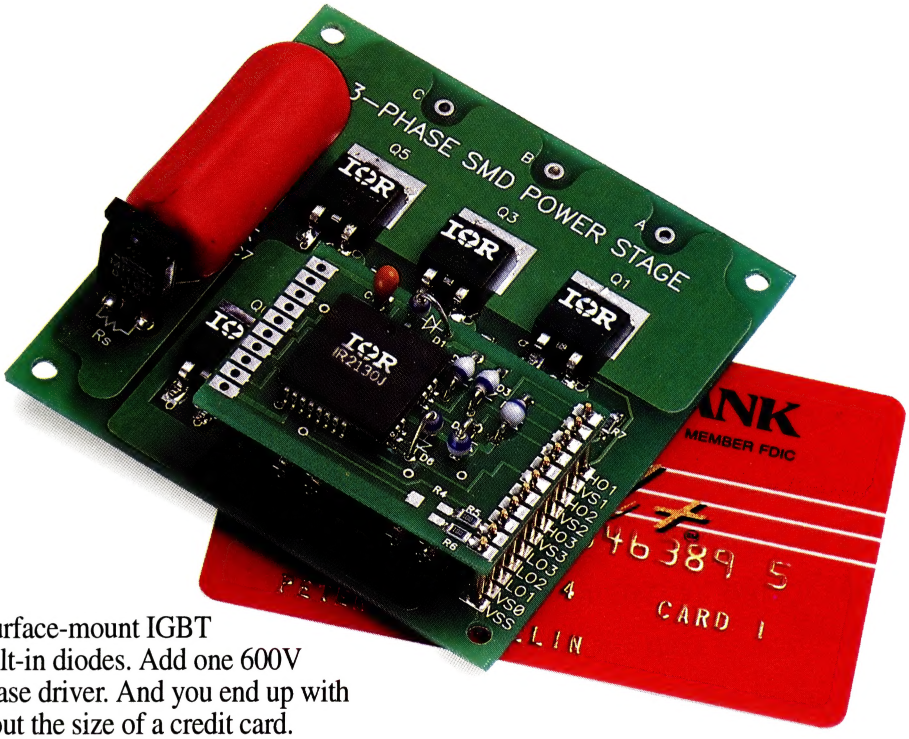

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